COM Express

2013

EXTREME RUGGED

At ADLINK, We CARE

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TECHNOLOGY INC.

Technical Leadership & Membership

- Intel Intelligent Systems Alliance Associate Member
- PICMG Executive Member
- PC/104 Embedded Consortium Affiliate Member
- SFF-SIG Voting Member
- PXISA Sponsor Member
- AXIe Consortium Strategic Member
- Montavista Partner
- Wind River Hardware Partner
- Automation Imaging Association Member
- Microsoft Windows Embedded Partner

"ADLINK is a leader in technical advancements in embedded computing, test & measurement, industrial automation and communication technology. We provide high-quality and long-term solutions for telecom, intelligent transportation, and electronic manufacturing industries."

Jeff Munch, ADLINK Chief Technical Officer
Chairman of PICMG ATCA and COM Express subcommittees

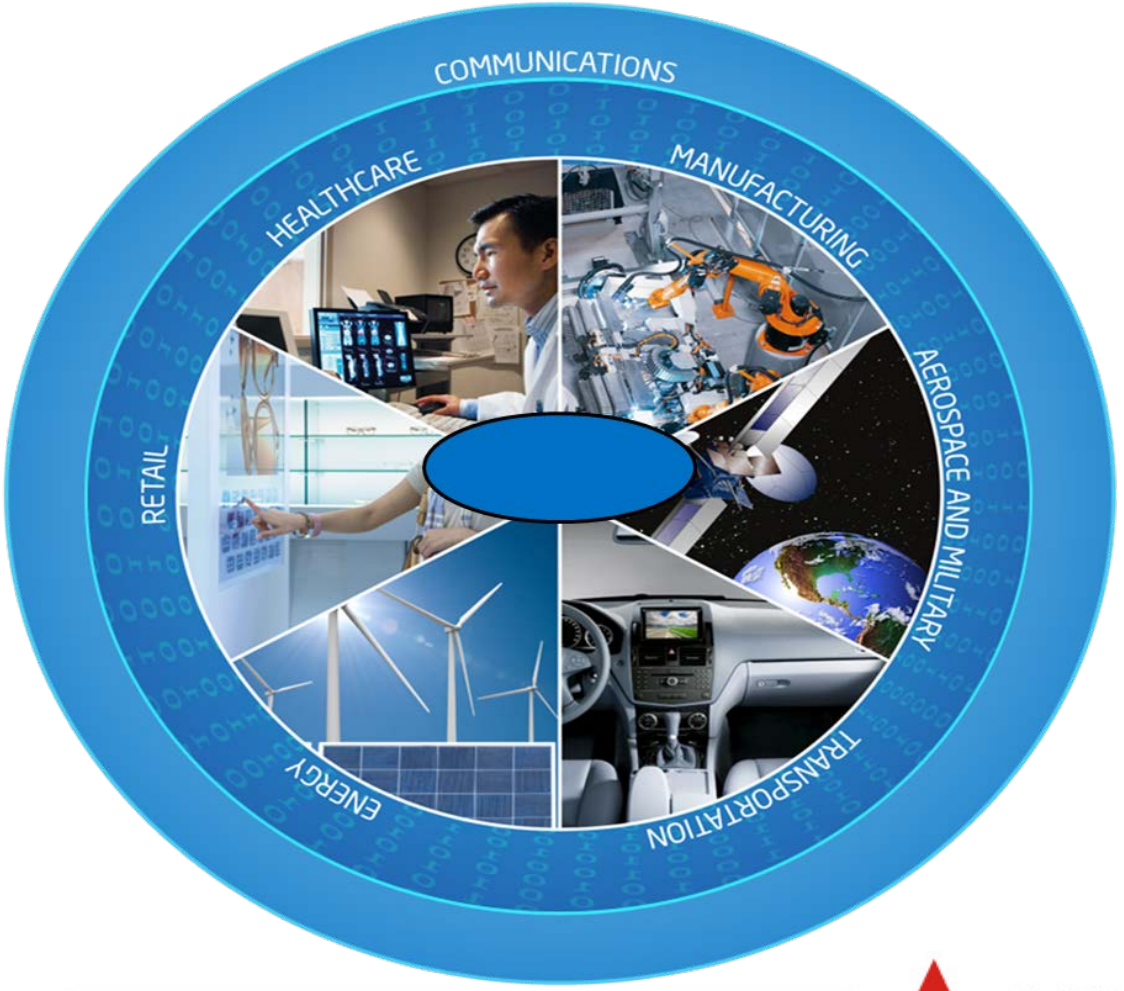
AdvancedTCA® AdvancedMC™ CompactPCI® COM Express ETX® PC/104

"AXIe's next-generation industrial standard dramatically improves scalability and performance for instrumentation and semiconductor testing products and systems. ADLINK is committed to providing our customers with the most modular and flexible products, empowering significant reductions in development and unit costs."

- Roy Wan, ADLINK Chief Director of
Measurement and Automation Product Segment
Member of the Board of AXIe Consortium Strategic Member

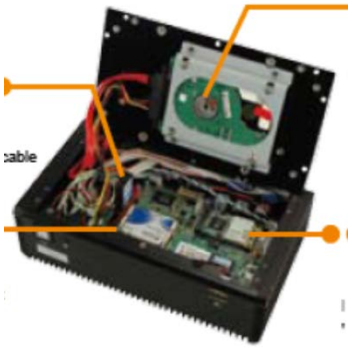
Proliferation of Compute Functions

- Transportation
  - Data Collection
- Energy
  - Monitoring
- Medical
  - Control



What are the Compute Options

- Motherboard
  - Ruggedization
    - Add in cards……
  - Shock + Vib / Operating temperature
  - Life cycle
- Grow your own
- Use industry standard compute engines

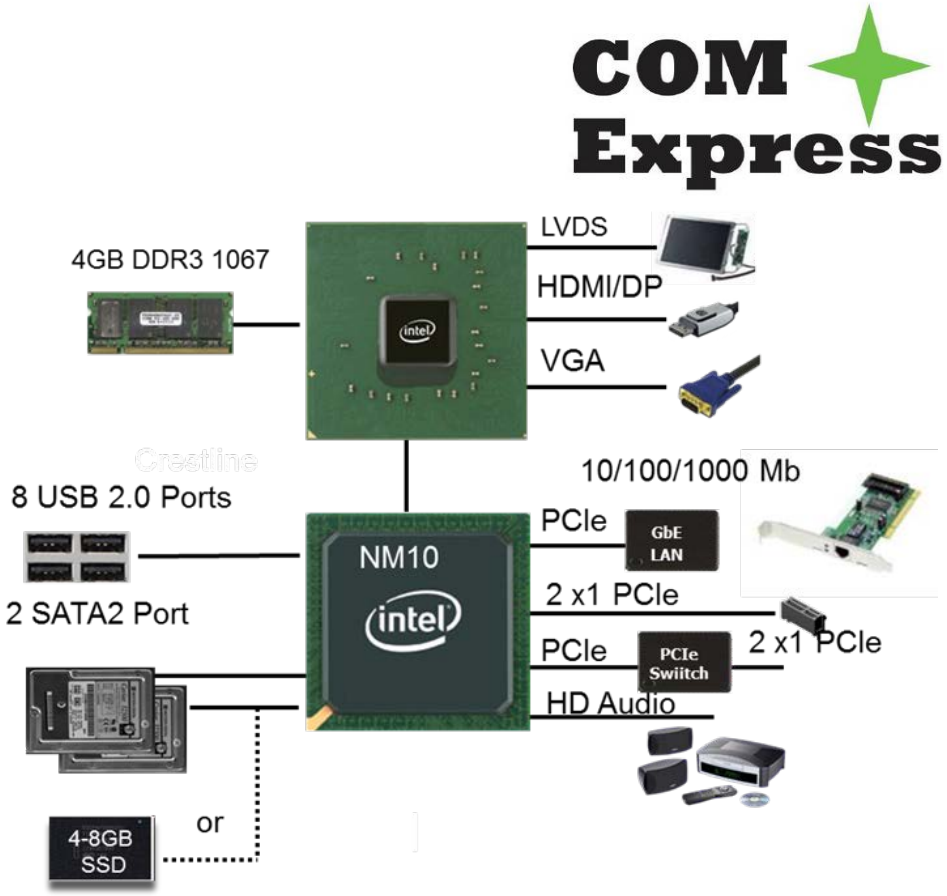


Industry Standard Compute Engines

- Focus on your core competency – use an existing standard based product
  - PC/104
  - Computer on Module
    - COM Express
    - SMARC

COM Express

- CPU + chipset + memory on a module
- High speed interfaces localized
- Carrier board contains relevant I/O connections and customizations
- Ability to ruggedize off card connections
- Add application specific I/O to the carrier board



PICMG and COM Express Subcommittee

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What is PICMG

- The PICMG (PCI Industrial Computer Manufacturers Group) is a consortium of over 250 companies who collaboratively develop specifications that adapt PCI technology for use in industrial and telecommunications computing applications.

History of PICMG

- Founded in 1994, PICMG's original mission was to extend the PCI standard, from the PCI Special Interest Group for use in non-traditional computer markets such as Industrial Automation, Medical, Military and Telecom
- PICMG developed and maintains several specifications including:
  - CompactPCI®, AdvancedTCA®, AdvancedMC™, CompactPCI® Express, COM Express® and SHB Express®

What is COM Express

- COM Express, a computer-on-module (COM) form factor, is a highly integrated and compact PC that can be used in a design application much like an integrated circuit component.
- The COM Express standard is defined and owned by the PICMG (PCI Industrial Computer Manufacturers Group)

COM Express R2

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COM Express History

- Initial release 2005
  - Feature set focused on peripherals found in typical x86 design with 855GME class CPU
- Revision 2.0 2010
- Revision 2.1 2012

Why R2.0?

- Recent CPUs added new / faster interfaces
  - Digital Display Interface
  - SATA Gen 3
  - PCIe Gen 3
  - SuperSpeed USB 3.0
- Some legacy interfaces removed
  - PCI, PATA
- Other change requests
  - 95 x 95mm; 84x55mm module, Serial ports
  - Common software interface for common functions
    - Watchdog, I2C, flat panel control

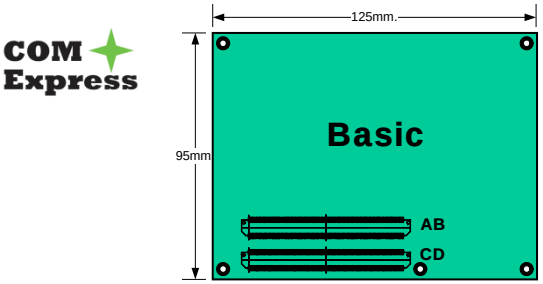
Changes in R2.0

- Added 2 new module types
  - Type 6 (dual connector)
  - Type 10 (single connector)
- Type 6
  - Added 3 Digital Display Interfaces that support DVI/HDMI/SDVO
  - Added USB 3.0 SupserSpeed USB
  - Removed PCI and PATA
- All Types
  - Added 2 serial ports,
  - Added PCIe Gen2/3 signaling
  - Added fan tachometer and SDIO signals
  - Added 95x95mm, 84x55mm module sizes
  - Defined a set of APIs

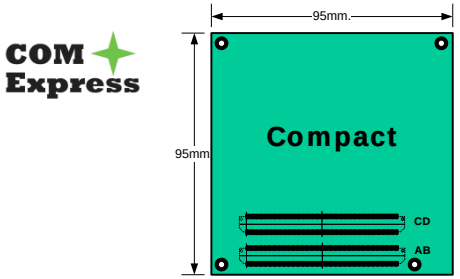
COM Express Sizes

Basic, and Compact

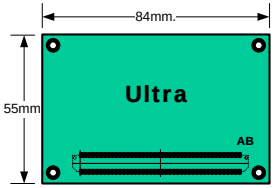
- **Basic** **125 x 95**



- **Compact** **95 x 95**



- **Mini** **84 x 55**



Digital Display Interface Mapping

	Pin Name	Type 6 Pin Number	SDVO	DP	HDMI/DVI (TMDS Signaling)
DDI 1	DDI1_PAIR0+	D26	SDVO1_RED+	DP1_LANE0+	TMDS1_DATA2+
	DDI1_PAIR0-	D27	SDVO1_RED-	DP1_LANE0-	TMDS1_DATA2-
	DDI1_PAIR1+	D29	SDVO1_GRN+	DP1_LANE1+	TMDS1_DATA1+
	DDI1_PAIR1-	D30	SDVO1_GRN-	DP1_LANE1-	TMDS1_DATA1-
	DDI1_PAIR2+	D32	SDVO1_BLU+	DP1_LANE2+	TMDS1_DATA0+
	DDI1_PAIR2-	D33	SDVO1_BLU-	DP1_LANE2-	TMDS1_DATA0-
	DDI1_PAIR3+	D36	SDVO1_CK+	DP1_LANE3+	TMDS1_CLK+
	DDI1_PAIR3-	D37	SDVO1_CK-	DP1_LANE3-	TMDS1_CLK-
	DDI1_PAIR4+	C25	SDVO1_INT+		
	DDI1_PAIR4-	C26	SDVO1_INT-		
	DDI1_PAIR5+	C29	SDVO1_TVCLKIN+		
	DDI1_PAIR5-	C30	SDVO1_TVCLKIN-		
	DDI1_PAIR6+	C15	SDVO1_FLDSTALL+		
	DDI1_PAIR6-	C16	SDVO1_FLDSTALL-		
	DDI1_HPD	C24		DP1_HPD	HDMI1_HPD
	DDI1_CTRLCLK_AUX+	D15	SDVO1_CTRLCLK	DP1_AUX+	HMDI1_CTRLCLK
	DDI1_CTRLDATA_AUX-	D16	SDVO1_CTRLDATA	DP1_AUX-	HMDI1_CTRLDATA
	DDI1_DDC_AUX_SEL	D34			

Digital Display Interface

- Leverages VESA DisplayPort Interoperability Guideline http://www.vesa.org/Standards/free.htm.

Module	Carrier / Cable Adapter Requirements	Destination
DP Only	None - Straight through to DP receptacle	DisplayPort
	N/A – not a valid combination	DVI/HDMI
DVI/HDMI	N/A – not a valid combination	DisplayPort
	None - Straight through to DVI/HDMI receptacle	DVI/HDMI
Dual Mode	None - Straight through to DP receptacle	DisplayPort
	Level shifters on data and DDC before DVI/HDMI connector	DVI/HDMI

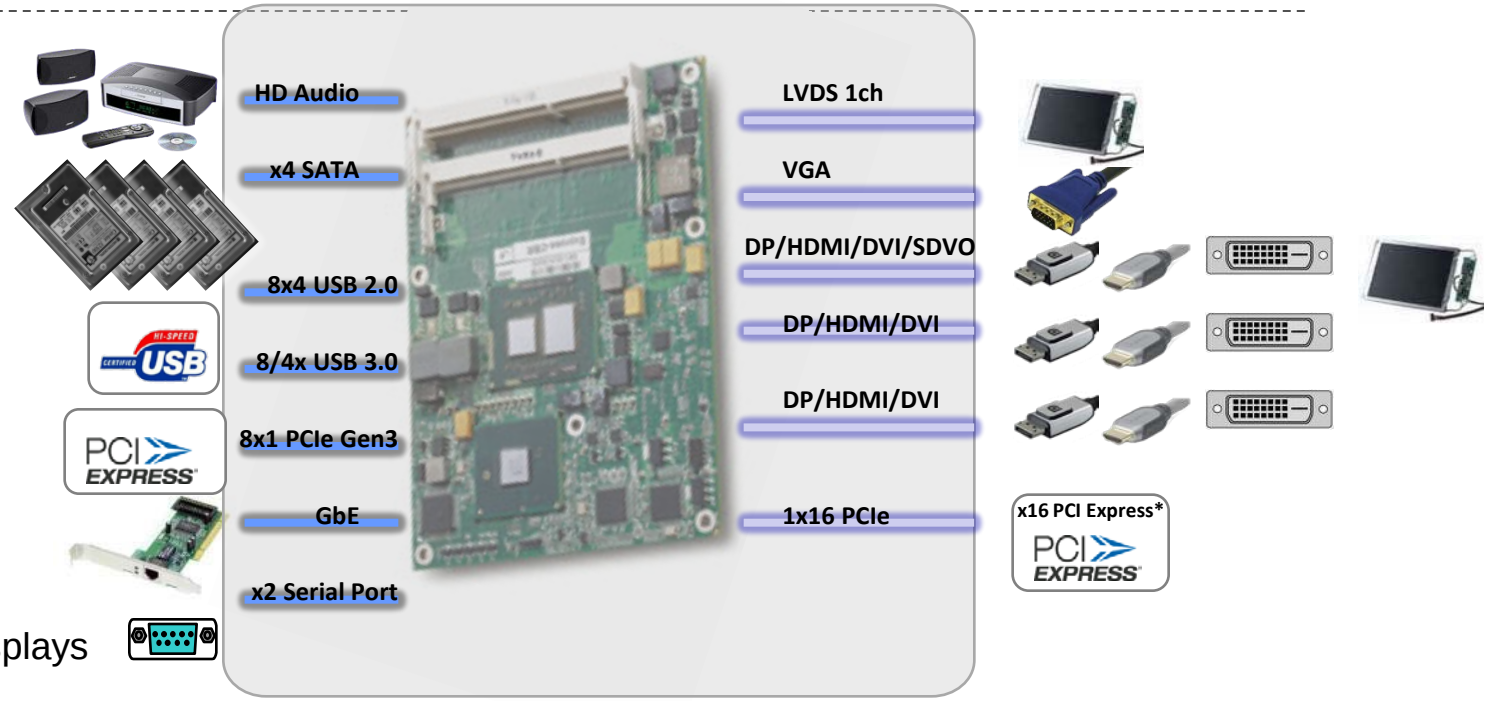
SuperSpeed USB 3.0

- SS USB adds a tx and rx pair to the standard USB interface
- COM.0 R1.0 supports 8 USB ports. R2.0 allows 4 of those ports to support SS USB by allocating 32 pins
- Pins are allocated but no design rules since SS silicon does not yet exist
- The 32 pins are from the PATA interface

COM Express Type 6 Interfaces

Type 6 Features

- Video
  - x3 DDI
    - Display Port
    - HDMI
    - DVI
    - SDVO (x1)
  - VGA
  - LVDS 1ch
  - 1x16 PCI Express
  - Drive 3 independent displays
- I/O
  - Audio
  - 4 SATA
  - 8 /4USB 2.0/3.0
  - 8 x1 PCI Express Gen 3
  - GbE
  - 2 Serial Ports



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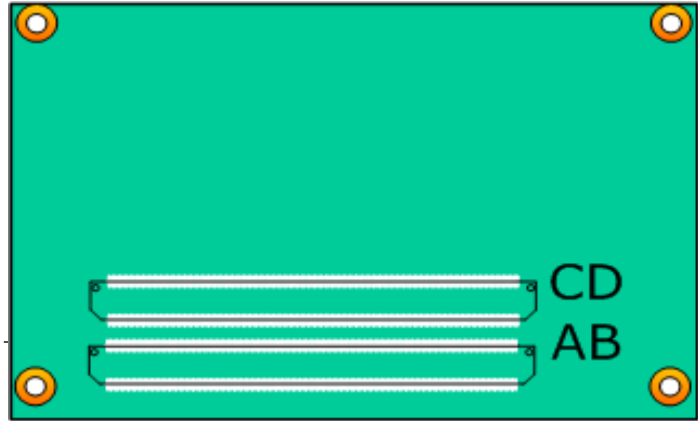
Type 2 and Type 6 Feature Comparison



Type 6

D	4x USB 3.0	2x PCIe x1	3x DDI (SDVO/HDMI/DVI)	PEG PCIe x16								12V
C												
B	LPC Bus	4x SATA	Audio	8x USB2.0	6x PCIe x1	LVDS Channel B	CRT	FAN & SPI select	Control & Miscella neous	5Vsb	12V total amount of pins reduced	
A	GbE LAN					LVDS Channel A	Control & Miscellaneous			SPI 2 Serial TPM, Type ID		

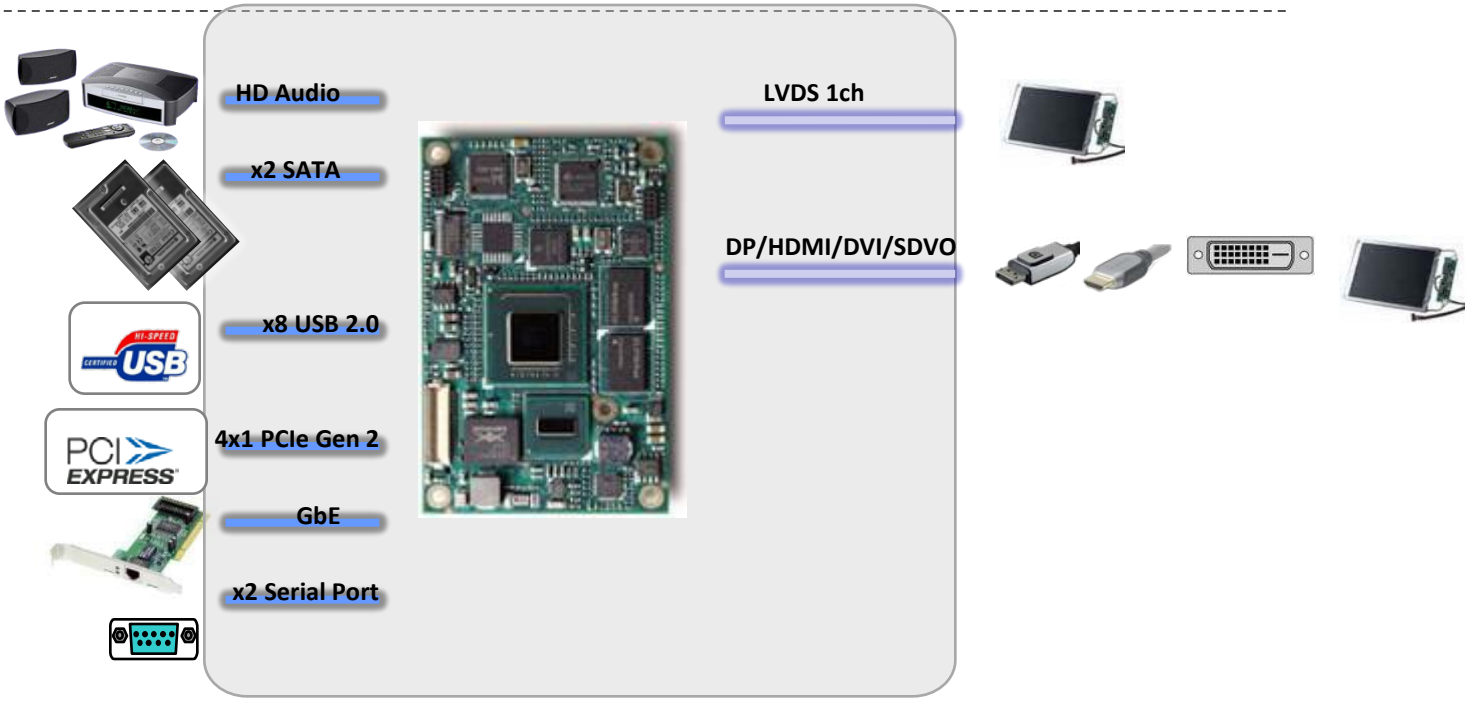
Type 2

D	PATA	32 bit PCI	PEG/SDVO PCIe x16								12V
C											
B	LPC Bus	4x SATA	Audio	8x USB2.0	6x PCIe x1	LVDS Channel B	CRT	SPI select	Control & Miscella neous	5Vsb	12V
A	Gbe LAN					LVDS Channel A	Control & Miscellaneous			SPI & Type ID	

COM Express Type 10 Interfaces

Type 10 Features

- Video
  - x1 DDI
    - Display Port
    - HDMI
    - DVI
    - SDVO (x1)
  - LVDS 1ch
- I/O
  - Audio
  - 2 SATA
  - 8 USB 2.0
  - 4 x1 PCI Express Gen 2
  - GbE
  - 2 Serial Ports



Type 10 Carrier

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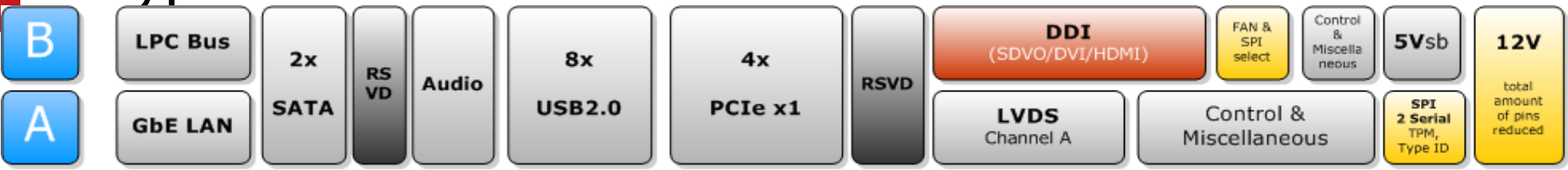
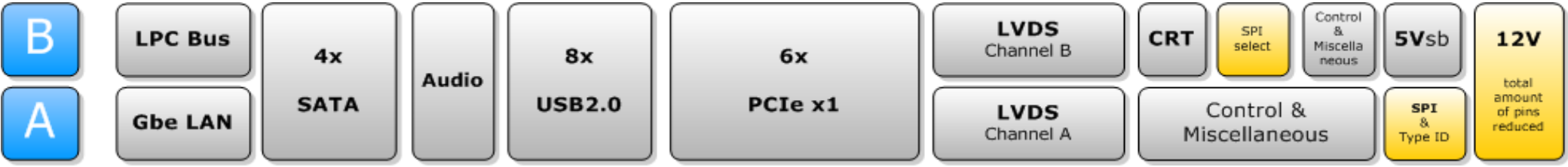
Type 1 and Type10 Feature Comparison

Type 10



Type 1



Common Features: 2xSATA, GbE, 8xUSB 2.0, 4xPCIe, LVDS, Audio

Embedded Application Programming Interface

- EAPI helps abstract vendor specific hardware
- Provides a set of APIs for
  - System information
  - Watchdog timer
  - I2C Bus
  - Flat panel brightness control
  - GPIO control
  - User data storage

```
uint32_t
EAPI_CALLTYPE
EApiVgaSetBacklightEnable(
    __IN  uint32_t  Id      , /* Backlight Id */
    __IN  uint32_t  Enable    /* Backlight Enable */
    );
```

COM.0 R2 Observations

- It is possible to design a carrier that can support Type 6/2 or 1/10 but there will be a limitation on video
- Chipset manufacturers are removing support for SDVO, VGA, and LVDS. Migrate to DisplayPort and Embedded Display Port
- R2.0 does not obsolete R1.0 designs. Major effort went into maintaining backwards compatibility

COM.0 Next Steps

- Standards are good for 5-10 years
- COM.0 R2.1 was released in 2012 – next iteration expected to start 2016 with a 2017 release
- COM Express Carrier Design Guide R2.0
  - In final ballot stage
  - Includes schematic examples for COM Express R2.0 and R2.1

Common Carrier Issues

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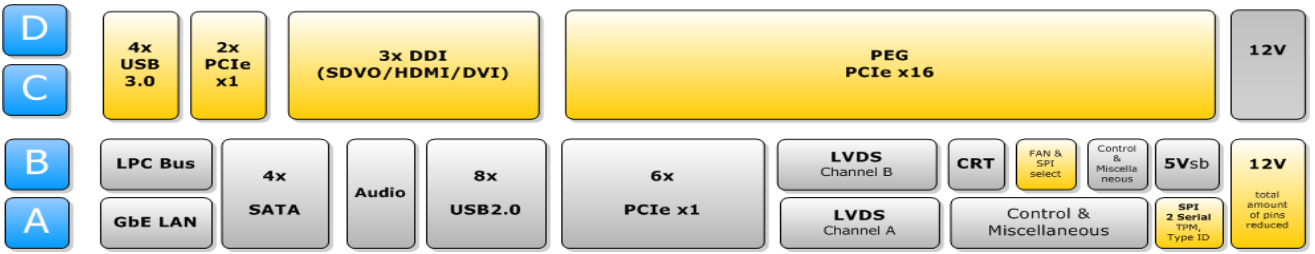
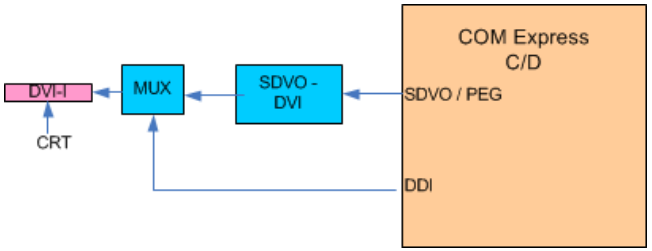
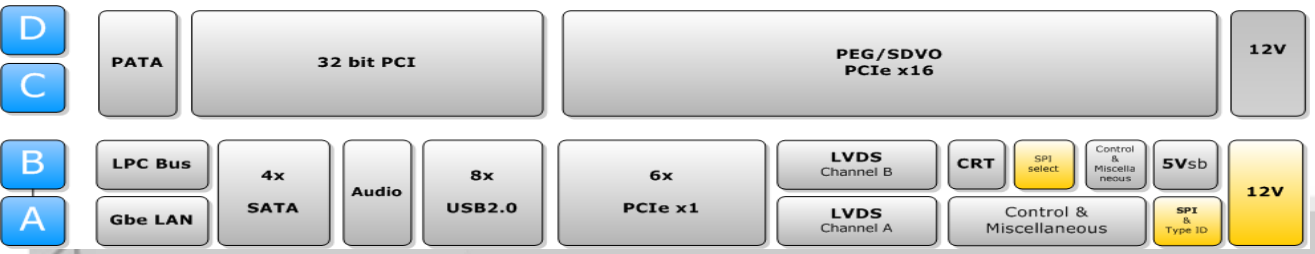
Designing for Type 2 and Type 6

- Do not use PCI, IDE, or SDVO
- VGA video, LVDS common
- DDI (HDMI/DVI) is a challenge, but possible
  - LVDS -> HDMI possible……

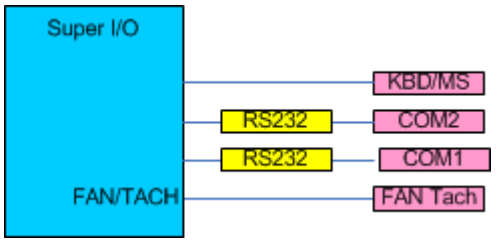






Serial Ports

- Super I/O on LPC bus common way to add serial ports
- Often a need for serial console during POST/BOOT
- Type 6 modules support serial port directly
- Requires BIOS support that is S(I/O) specific….
- Contact your COM vendor……



USB Ports

- Support for Wake on USB
- USB often powered by a switch 5V
- Support for Wake On requires that the device be powered during sleep states
- Use 5V Standby

Back feeding of Power

- There are typically two power domains
  - Standby and non-standby
- “Good” design practice would have the carrier board provide pull-ups on device inputs to prevent floating signals
- The pull-ups can provide leakage path for power
- Follow the COM Express guide for pull-up locations

The Module ***shall*** provide the termination for the signals below. The following signals ***should*** be pulled-up to 3.3V with a 10kΩ resistor

- KBD_A20GATE
- KBD_RST#
- BIOS_DIS[0:1]#
- EXCD[0:1]_CPPE#
- FAN_TACHIN

Back feeding of Power – Not so Obvious

- Carrier controls power to module
- Carrier actively drives a signal to the module
- Receiving IC on module contains ESD clamping diodes

- Clamping diodes provide a leakage path that can drive power rails on a module to invalid levels
- Pay attention to the “Pwr Rail” column in the COM.0 spec

I2C Bus	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
I2C_CK	I/O OD CMOS	3.3V Suspend/ 3.3V	General purpose I^2C port clock output	All
I2C_DAT	I/O OD CMOS	3.3V Suspend/ 3.3V	General purpose I^2C port data I/O line	All

Power Supplies

- A Carrier design can be powered different ways
  - "ATX" power button activated, standby power
  - "AT" power switch
  - Single input
- Supporting sleeps states requires a clear understanding of the Modules "S" states and what should be powered when
- The ability of the OS to shutdown power to the module….

Power and System Management	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
PWRBTN#	I CMOS	3.3V Suspend/ 3.3V	Power button to bring system out of S5 (soft off), active on falling edge.	All
SYS_RESET#	I CMOS	3.3V Suspend/ 3.3V	Reset button input. Active low request for module to reset and reboot. May be falling edge sensitive. For situations when SYS_RESET# is not able to reestablish control of the system, PWR_OK or a power cycle may be used.	All
CB_RESET#	O CMOS	3.3V Suspend/ 3.3V	Reset output from Module to Carrier Board. Active low. Issued by Module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the Module software.	All
PWR_OK	I CMOS	3.3V / 3.3V	Power OK from main power supply. A high value indicates that the power is good. This signal can be used to hold off Module startup to allow carrier based FPGAs or other configurable devices time to be programmed.	All
SUS_STAT#	O CMOS	3.3V Suspend/ 3.3V	Indicates imminent suspend operation; used to notify LPC devices.	All
SUS_S3#	O CMOS	3.3V Suspend/ 3.3V	Indicates system is in Suspend to RAM state. Active low output. An inverted copy of SUS_S3# on the Carrier Board may be used to enable the non-standby power on a typical ATX supply.	All
SUS_S4#	O CMOS	3.3V Suspend/ 3.3V	Indicates system is in Suspend to Disk state. Active low output.	All
SUS_S5#	O CMOS	3.3V Suspend/ 3.3V	Indicates system is in Soft Off state.	All
WAKE0#	I CMOS	3.3V Suspend/ 3.3V	PCI Express wake up signal.	All
WAKE1#	I CMOS	3.3V Suspend/ 3.3V	General purpose wake up signal. May be used to implement wake-up on PS2 keyboard or mouse activity.	All
BATLOW#	I CMOS	3.3V Suspend/ 3.3V	Indicates that external battery is low. This port provides a battery-low signal to the Module for orderly transitioning to power saving or power cut-off ACPI modes.	All
LID#	I OD CMOS	3.3V Suspend/ 12V	LID button. Low active signal used by the ACPI operating system for a LID switch.	T6, T10
SLEEP#[12]	I OD CMOS	3.3V Suspend/ 12V	Sleep button. Low active signal used by the ACPI operating system to bring the system to sleep state or to wake it up again.	T6, T10

Resources

- PICMG Carrier Design Guide
  - Reference schematics for all interfaces
  - http://www.picmg.org

Thank You

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