DAQ/DAQe/PXI-250x Series

High Performance
Analog Output Multi-function Cards

User's Manual

Manual Rev. 1.0
Revision Date: Dec. 29, 2023
Part No: 50M-12264-1000

LEADING EDGE COMPUTING

Revision History

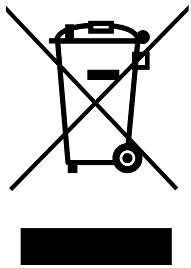
Revision	Release Date	Description of Change(s)
2.01	2006-12-21	Previous release PN: 50-12265-100
1.0	2023-12-29	▶ Initial release under new part number. ▶ Added 1.4 Software Support. ▶ Added 2.4 Switch and Jumper Settings. ▶ Added SSI connector pin assignment on PXI J2. ▶ Added 4.1.6 Bus-mastering DMA Data Transfer.

Preface

Disclaimer

The information in this document is subject to change without prior notice in order to improve reliability, design, and function and does not represent a commitment on the part of the manufacturer.

In no event will the manufacturer be liable for direct, indirect, special, incidental, or consequential damages arising out of the use or inability to use the product or documentation, even if advised of the possibility of such damages.



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Battery Labels (for products with battery)

California Proposition 65 Warning

WARNING: This product can expose you to chemicals including acrylamide, arsenic, benzene, cadmium, Tris(1,3-dichloro-2-propyl)phosphate (TDCPP), 1,4-Dioxane, formaldehyde, lead, DEHP, styrene, DINP, BBP, PVC, and vinyl materials, which are known to the State of California to cause cancer, and acrylamide, benzene, cadmium, lead, mercury, phthalates, toluene, DEHP, DIDP, DnHP, DBP, BBP, PVC, and vinyl materials, which are known to the State of California to cause birth defects or other reproductive harm. For more information go to www.P65Warnings.ca.gov**.**

Trademarks

Product names mentioned herein are used for identification purposes only and may be trademarks and/or registered trademarks of their respective companies.

Conventions

Take note of the following conventions used throughout this manual to make sure that users perform certain tasks and instructions properly.

NOTE:	Additional information, aids, and tips that help users perform tasks.

CAUTION:	Information to prevent ***minor*** physical injury, component damage, data loss, and/or program corruption when trying to complete a task.

WARNING:	Information to prevent ***serious*** physical injury, component damage, data loss, and/or program corruption when trying to complete a specific task.

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1 Introduction

The DAQ/DAQe/PXI-250x Series is an advanced analog output card based on the 32-bit PCI/PXI architecture. High performance designs and state-of-the-art technology make this card ideal for waveform generation, industrial process control, and signal analysis applications in medical, process control, etc.

1.1 Features

DAQ/DAQe/PXI-250x Series advanced analog output cards provide the following advanced features:

- 32-bit PCI/PXI-Bus, plug and play
- Up to 1MS/s analog output rate
- Up to 400KS/s analog input rate
- Up to 8 analog output channels for DAQ/DAQe/PXI-2502, and 4 analog output channels for DAQ/DAQe/PXI-2501
- Up to 4 analog input channels for DAQ/DAQe/PXI-2502, and 8 analog input channels for DAQ/DAQe/PXI-2501
- Programmable bipolar/unipolar range for analog input channels and individual analog output channels
- Programmable internal/external reference for individual analog output channels
- D/A FIFO size: 8K samples for DAQ/DAQe/PXI-2501, and 16K samples for DAQ/DAQe/PXI-2502
- A/D FIFO size: 2K samples
- Versatile trigger sources: software trigger, external digital trigger, ana-log trigger and trigger from System Synchronization Interface (SSI)
- A/D Data transfer: software polling & bus-mastering DMA with Scat-ter/Gather
- D/A Data transfer: software update and bus-mastering DMA with Scatter/Gather
- A/D trigger modes: post-trigger, delay-trigger with re-trigger functionality
- D/A outputs with waveform generation capability
- System Synchronization Interface (SSI)
- A/D and D/A fully auto-calibration
- Built-in programmable D/A external reference voltage compensator
- Completely jumper-less and software configurable

1.2 Applications

- Automotive Testing
- Arbitrary Waveform Generator
- Transient signal measurement
- ATE
- Laboratory Automation
- Biotech measurement

1.3 Specifications

Analog Input (AI)

- Number of channels:
  - 4 single-ended for DAQ/DAQe/PXI-2502
  - 8 single-ended for DAQ/DAQe/PXI-2501
- AD converter: LTC1416
- Max sampling rate: 400KS/s
- Resolution: 14 bits
- FIFO buffer size: 2K samples
- Input range: Bipolar: ±10V, unipolar: 0~10V
- Over voltage protection: Continuous ±35V maximum
- Input impedance: 1GΩ | 6pF
- Trigger modes: Pre-trigger, post-trigger, middle-trigger, and delay trigger
- Data transfers: Programmed I/O, and bus-mastering DMA with scatter/gather
- Input coupling: DC
- Offset error: ±4mV max
- Gain error: ±0.3 % of output max

Analog Output (AO)

- Number of channels: 4-ch for DAQ/DAQe/PXI-2501, 8-ch for DAQ/DAQe/PXI-2502
- DA converter: AD7945
- Max update rate: 1MS/s
- Resolution: 12 bits
- FIFO buffer size: 8K for DAQ/DAQe/PXI-2501, 16K for DAQ/PXI- 2502
- Data transfer: Programmed I/O, and bus-mastering DMA with scat-ter/gather
- Voltage reference: internal 10V or external up to ±510V
- Output range:
  - Bipolar: ±10V or ±external reference
  - Unipolar: 0~10V or 0~ external reference
- Settling time for –10~+10V step: 2μs
- Slew rate: 20V/μs
- Output coupling: DC
- Protection: Short-circuit to ground
- Output impedance: 0.1Ω. max.
- Output current: ±5mA max.
- Power-on state: 0V steady-state
- Power-on glitch: ±600mV/500μs
- Offset error: ±2mV max
- Gain error: ±0.05% of output max

General Purpose Digital I/O (G.P. DIO)

- Number of channels: 24 programmable Input/Output
- Compatibility: TTL/CMOS
- Input voltage:
  - C> Logic Low: VIL=0.8V max.; IIL=0.2mA max.
  - C> High: VIH=2.0V max.; IIH=0.02mA max
- Output voltage:
  - C> Low: VOL=0.5 V max.; IOL=8mA max.
  - C> High: VOH=2.7V min; IOH=400?A

General Purpose Timer/Counter (GPTC)

- Number of channel: 2 Up/Down Timer/Counters
- Resolution: 16 bits
- Compatibility: TTL/CMOS
- Clock source: Internal or external
- Max source frequency: 10MHz

Analog Trigger (A.Trig)

- Source: external analog trigger (EXTATRIG)
- Level: ±10V external
- Resolution: 8 bits
- Slope: Positive or negative (software selectable)
- Hysteresis: Programmable
- Bandwidth: 400khz
- External Analog Trigger Input (EXTATRIG)
- Input Impedance: 40kΩ
- Coupling: DC
- Protection: Continuous ±35V maximum

System Synchronous Interface (SSI)

- Trigger lines: 7

Calibration

- Recommended warm-up time: 15 minutes
- Onboard reference: 5.0V
- Temperature coefficient: ±2ppm/°C
- Long-term stability: 6ppm/1000Hr

Physical

- Dimensions: 175mm by 107mm
- I/O connector: 68-pin female mini-SCSI type
- Power Requirement: +5VDC: 1.6A typical

Operating Environment

- Ambient temperature: 0 to 55°C
- Relative humidity: 10% to 90% non-condensing

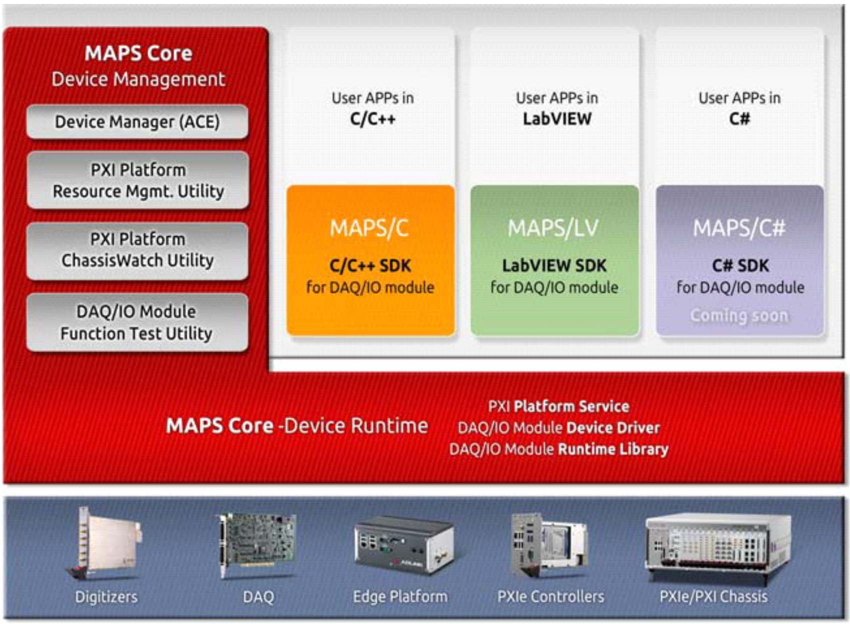
Storage Environment

- Ambient temperature: -20 to 70°C
- Relative humidity: 5% to 95% non-condensing

1.4 Software Support

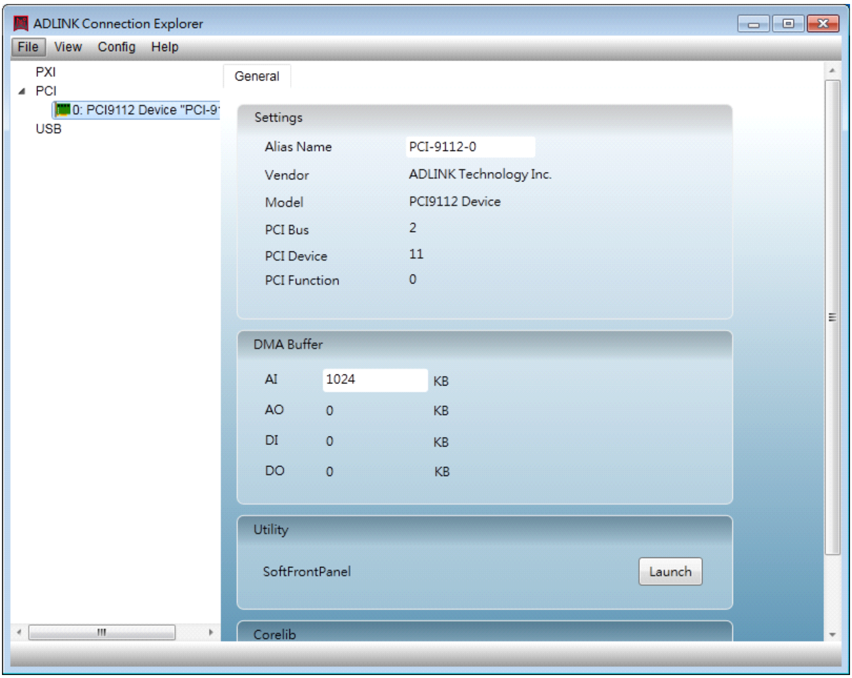
ADLINK provides versatile software drivers and packages to suit various user approaches to building a system. Aside from programming libraries, such as DLLs, for most Windows-based systems, ADLINK also provides drivers for other application environments such as LabVIEW. All software can be downloaded from the ADLINK official website. Commercial software drivers are protected with licensing authorization codes. Without an authorization code, you can install and run the demo version for trial/demonstration purposes for up to two hours. Contact your ADLINK dealer to purchase a software license. ADLINK Measurement, Automation & Platform Service (MAPS) is a software service package designed for data acquisition, automation and PXI platforms.

By leveraging low-level kernel management and a user friendly API, users can easily manage devices under a Windows environment and focus on developing applications.

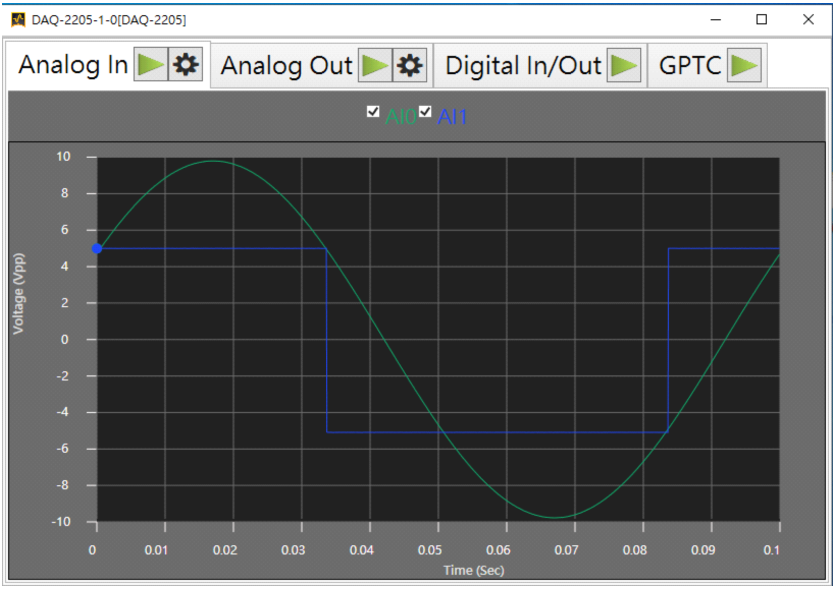


1.4.1 MAPS Core

ADLINK MAPS Core is a software package that includes all the device drivers for Windows and a system level management tool called ACE (ADLINK Connection Explorer). With MAPS Core installed, the operating system can identify ADLINK devices and assign the necessary resources for low-level access, such as IO read/write or direct memory access. MAPS Core is necessary for all ADLINK DAQ modules. To ensure the user has the latest software, go to the ADLINK product webpage or contact ADLINK technical service. MAPS Core also comes with a system management portal called ADLINK Connection Explorer (ACE). Through ACE, users can discover and manage ADLINK DAQ modules to reserve a certain size of memory buffer for DMA operation or set the user alias name for operating the module in a LabVIEW environment.



ADLINK Connection Explorer (ACE) also provides a ready-to-use soft-front panel for digitizer products. Clicking the Launch button in the "Utility" block allows users to control digitizers through the UI and display the acquired waveform/data on the screen.



1.4.2 MAPS/LV, LabVIEW Support

Customers who develop their own programs in LabVIEW must install the MAPS/LV software package. MAPS/LV, also called DAQ-LabVIEW Plus, includes the software library and sample program for LabVIEW. For more information, download and install the latest MAPS/LV software from the following website and refer to the MAPS/LV manual:

https://www.adlinktech.com/Products/Data_Acquisition/DAQSoftware_Utility/MAPS_LV

1.4.3 MAPS/C, C & C++ Support

Customers who develop their own programs in C or C++ environments must install the MAPS/C software package. MAPS/C includes all the software components required for developing applications in C/C++, such as header files, a device API library and versatile sample programs for understanding how to manipulate the device correctly. Find the latest MAPS/C on the ADLINK website.

https://www.adlinktech.com/Products/Data_Acquisition/DAQSoftware_Utility/MAPS_C

2 Installation

This chapter describes how to install DAQ/DAQe/PXI-250x Series cards. The contents of the package and unpacking information that you should be aware of are outlined first.

2.1 Contents of Package

In addition to this User's Guide, the package should include the following items:

- DAQ/DAQe/PXI-250x Series Multi-function Data Acquisition Card
- Software Installation Guide

If any of these items are missing or damaged, contact the dealer from whom you purchased the product. Save the shipping materials and carton in case you want to ship or store the product in the future.

2.2 Unpacking

Your DAQ/DAQe/PXI-250x Series card contains electro-static sensitive components that can be easily be damaged by static electricity.

Therefore, the card should be handled on a grounded anti-static mat. The operator should be wearing an anti-static wristband, grounded at the same point as the anti-static mat.

Inspect the card module carton for obvious damages. Shipping and han-dling may cause damage to your module. Be sure there are no shipping and handling damages on the modules carton before continuing.

After opening the card module carton, extract the system module and place it only on a grounded anti-static surface with component side up.

Again, inspect the module for damages. Press down on all the socketed IC's to make sure that they are properly seated. Do this only with the module place on a firm flat surface.

You are now ready to install your DAQ/DAQe/PXI-250x Series.

Note: DO NOT APPLY POWER TO THE CARD IF IT HAS BEEN DAMAGED.

2.3 DAQ/DAQe/PXI-250x Series Layout

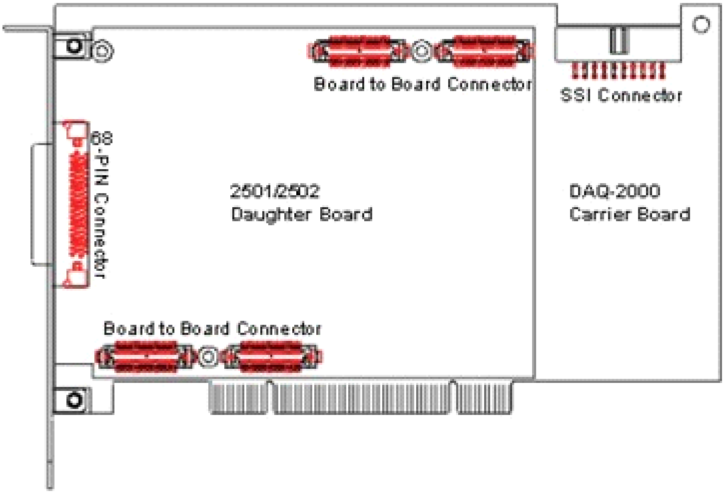


Figure 2-1: PCB Layout of the DAQ-2502/2501

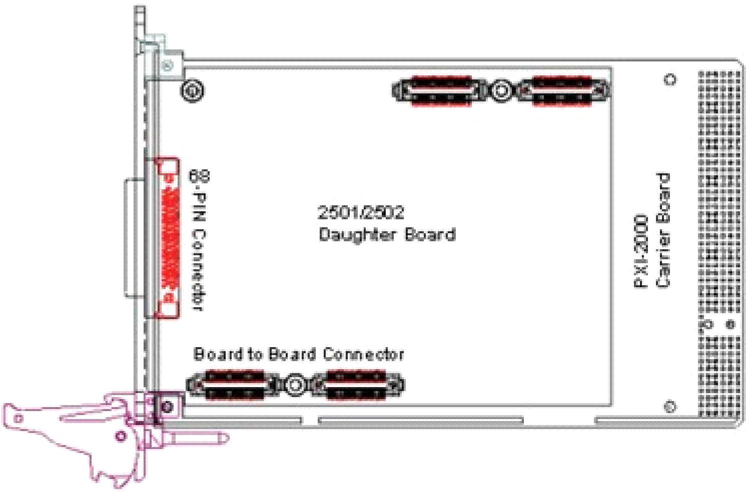


Figure 2-2: PCB Layout of the PXI-DAQ-2502/2501

2.4 Switch and Jumper Settings

2.4.1 Board ID (SW1)

The DAQ/DAQe/PXI-250x Series has a built-in DIP switch (SW1), which is used to define each card's board ID. When there are multiple cards on the same platform, this board ID switch is useful for identifying each card's device number. After setting each DAQ/DAQe/PXI-250x Series card, you can identify each card in the system with different device numbers. The default value of the Board ID is 0 and if you need to adjust it to another value, set the SW1 switch as shown in the table below.

Figure 2-3: Board ID SW1 DIP Switch

SW1	Pin 1	Pin 2	Pin 3	Pin 4
Board ID	**ID0**	**ID1**	**ID2**	**ID3**
0	Off	Off	Off	Off
1	On	Off	Off	Off
2	Off	On	Off	Off
3	On	On	Off	Off
4	Off	Off	On	Off
5	On	Off	On	Off
6	Off	On	On	Off
7	On	On	On	Off
8	Off	Off	Off	On
9	On	Off	Off	On
10	Off	On	Off	On
11	On	On	Off	On
12	Off	Off	On	On
13	On	Off	On	On
14	Off	On	On	On
15	On	On	On	On

Table 2-1: Board ID SW1 DIP Switch Settings

NOTE:

Board ID configuration is disabled by default. To enable Board ID configuration, install D2K-DASK and launch W2K_D2kUtil.exe in C:\ADLINK\D2K-DASK\Utility\. Select your Card Type and uncheck Ignore Board ID. See figure below.

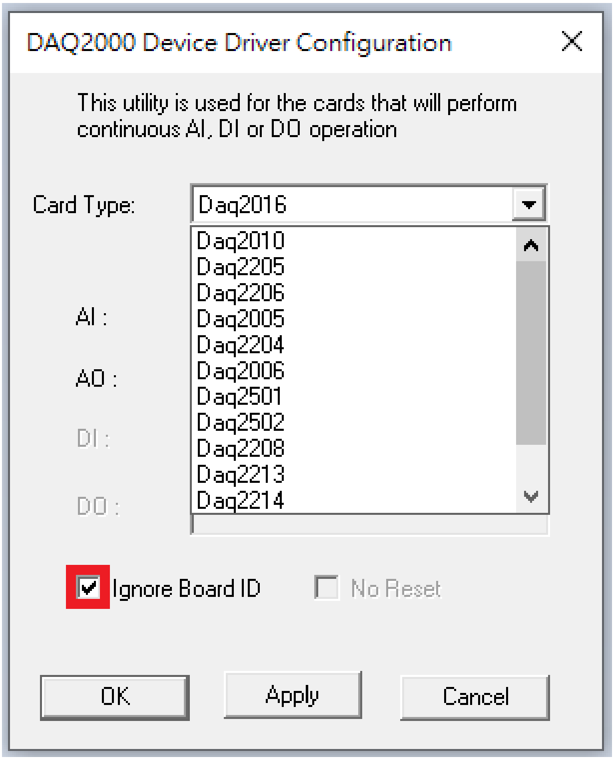
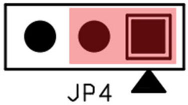
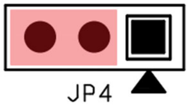


Figure 2-4: Enable Board ID Configuration

2.4.2 DIO Initial Status (JP4)

The default jumper setting is enabled, making the DIO initial status low by using a 1K ohm resistor poll down to GND. To disable this feature, move the jumper cap as shown in the table below.

Disabled	
Enabled	

2.5 PCI Configuration

1. Plug and Play:

As a plug and play component, the card requests an interrupt number via its PCI controller. The system BIOS responds with an interrupt assignment based on the card information and on known system parameters. These system parameters are determined by the installed drivers and the hardware load seen by the system.

2. Configuration:

The board configuration is done on a board-by-board basis for all PCI boards on your system. Because configuration is controlled by the system and software, there is no jumper setting required for base-address, DMA, and interrupt IRQ.

The configuration is subject to change with every boot of the sys-tem as new boards are added or removed.

3. Troubleshooting:

If your system doesn't boot or if you experience erratic operation with your PCI board in place, it's likely caused by an interrupt con-flict (perhaps the BIOS Setup is incorrectly configured). In general, the solution, once you determine it is not a simple oversight, is to consult the BIOS documentation that comes with your system.

3 Signal Connections

This chapter describes the connectors of the DAQ/DAQe/PXI-250x Series, and the signal connection between the DAQ/DAQe/PXI-250x Series and external devices.

3.1 Connectors Pin Assignment

DAQ/DAQe/PXI-250x Series is equipped with two 68-pin VHDCI-type connectors (AMP-787254-1). It is used for digital input / output, analog input / output, and timer/counter signals, etc. The pin assignments of the connectors are defined in the figures below.

AO_0	1	35	AGND
AO_1	2	36	AGND
AO_2	3	37	AGND
AO_3	4	38	AGND
AOEXTREF_A/AI_0	5	39	AGND
AI_1	6	40	AGND
EXTATRIG/AI_2	7	41	AGND
AOEXTREF_B/AI_3	8	42	AGND
AO_4/AI_4	9	43	AGND
AO_5/AI_5	10	44	AGND
AO_6/AI_6	11	45	AGND
AO_7/AI_7	12	46	AGND
AO_TRIG_OUTA	13	47	EXTWFTRG_A
AO_TRIG_OUTB	14	48	EXTWFTRG_B
GPTC1_SRC	15	49	VCC
GPTC0_SRC	16	50	DGND
GPTC0_GATE	17	51	GPTC1_GATE
GPTC0_OUT	18	52	GPTC1_OUT
GPTC0_UPDOWN	19	53	GPTC1_UPDOWN
RESERVED	20	54	DGND
AFI1	21	55	AFI0

Table 3-1: Connector CN1 pin assignment

PB7	22	56	PB6
PB5	23	57	PB4
PB3	24	58	PB2
PB1	25	59	PB0
PC7	26	60	PC6
PC5	27	61	PC4
DGND	28	62	DGND
PC3	29	63	PC2
PC1	30	64	PC0
PA7	31	65	PA6
PA5	32	66	PA4
PA3	33	67	PA2
PA1	34	68	PA0

Table 3-1: Connector CN1 pin assignment

Legend:

Pin #	Signal Name	Reference	Direction	Description
1~4	AO_<0..3>	AGND	Output	Voltage output of DA channel <0..3>
5	AOEXTREF_A/AI_0	AGND	Input	External reference for AO channel <0..3> / AI input 2
6	AI_1	AGND	Input	AI input 0
7	EXTATRIG/AI_2	AGND	Input	External analog trigger / AI input 1
8	AOEXTREF_B/AI_3	AGND	Input	External reference for AO channel <4..7> / AI input 3

Table 3-2: Connector CN2 pin assignment

Pin #	Signal Name	Reference	Direction	Description
9~12	AO_<4..7>/AI_<4..7>	AGND	Output/ Input	Voltage output of DA channel <4..7> / AI channel <4..7> (only for DAQ-2501)
13,14	AO_TRIG_OUT_<A,B>	DGND	Output	AO trigger signal for channel <0..3> <4..7>
15,16	GPTC<0,1>_SRC	DGND	Input	Source of GPTC<0,1>
17,51	GPTC<0,1>_GATE	DGND	Input	Gate of GPTC<0,1>
18,52	GPTC<0,1>_OUT	DGND	Input	Output of GPTC<0,1>
19,53	GPTC<0,1>_UPDOWN	DGND	Input	Up/Down of GPTC<0,1>
20	RESERVED	--------	--------	Reserved Pin
21,55	AFI<1,0>	DGND	Input	Auxiliary Function Input
22,56,23, 57,24,58, 25,59	PB<7,0>	DGND	PIO	Programmable DIO of 8255 Port B
26,60,27, 61,29,63, 30,64	PC<7,0>	DGND	PIO	Programmable DIO of 8255 Port C
31,65,32, 66,33,67, 34,68	PA<7,0>	DGND	PIO	Programmable DIO of 8255 Port A
35~46	AGND	--------	--------	Analog ground
47,48	EXTWFTRIG_<A,B>	DGND	Input	External waveform trigger for AO channel <0..3> <4..7>

Table 3-2: Connector CN2 pin assignment

Pin #	Signal Name	Reference	Direction	Description
49	VCC	DGND	Power (Output)	+5V Power Source
28,50,54, 62	DGND	--------	--------	Digital ground

Table 3-2: Connector CN2 pin assignment

*PIO means programmable I/O

SSI_TIMEBASE	1	2	DGND
SSI_ADCONV	3	4	DGND
SSI_DAWR	5	6	DGND
SSI_SCAN_START	7	8	DGND
RESERVED	9	10	DGND
SSI_AD_TRIG	11	12	DGND
SSI_DA_TRIG	13	14	DGND
RESERVED	15	16	DGND
RESERVED	17	18	DGND
RESERVED	19	20	DGND

Table 3-3: SSI connector pin assignment

SSI Connector Signal Description on PXI J2:

Sync. Signal	PXI J2 location	PXI Trigger Bus
SSI_TIMEBASE	B18	PXI_TRIG4
SSI_ADCONV	A16	PXI_TRIG1
SSI_SCAN_START	A18	PXI_TRIG3
SSI_AD_TRIG	C18	PXI_TRIG5
SSI_DAWR	A17	PXI_TRIG2
SSI_DA_START	B16	PXI_TRIG0
SSI_DA_TRIG	E18	PXI_TRIG6

Table 3-4: SSI Connector Pin Assignment on PXI J2

Legend:

SSI timing signal	Functionality
SSI_TIMEBASE	SSI master: send the TIMEBASE out SSI slave: accept the SSI_TIMEBASE to replace the internal TIMEBASE signal.
SSI_ADCONV	SSI master: send the ADCONV out SSI slave: accept the SSI_ADCONV to replace the internal ADCONV signal.
SSI_SCAN_START	SSI master: send the SCAN_START out SSI slave: accept the SSI_SCAN_START to replace the internal SCAN_START signal.
SSI_AD_TRIG	SSI master: send the internal AD_TRIG out SSI slave: accept the SSI_AD_TRIG as the digital trigger signal.
SSI_DAWR	SSI master: send the DAWR out. SSI slave: accept the SSI_DAWR to replace the internal DAWR signal.
SSI_DA_TRIG	SSI master: send the DA_TRIG out. SSI slave: accept the SSI_DA_TRIG as the digital trigger signal.

Table 3-5: Legend of SSI connector

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4 Operation Theory

The operation theories of the DAQ/DAQe/PXI-250x Series are described in this chapter. The functions include A/D conversion, D/A conversion, Digital I/O, and General Purpose Counter / Timer. This operation theory will help you understand how to configure and program the DAQ/DAQe/PXI-250x Series.

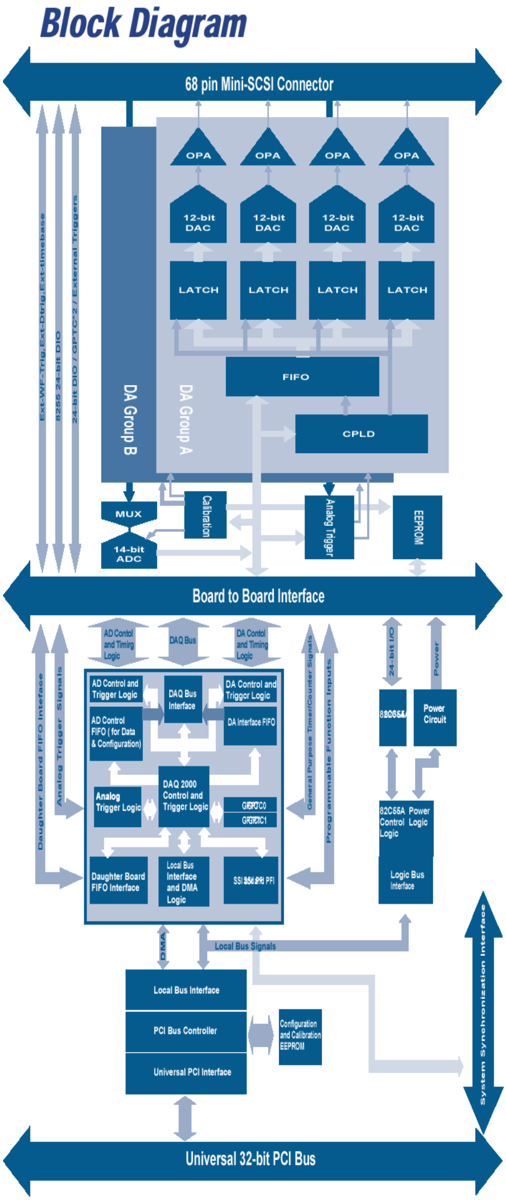


Figure 4-1: DAQ/DAQe/PXI-250x Series Block Diagram

4.1 A/D Conversion

When using an A/D converter, users should know the properties of the signal to be measured. In addition, users should setup the A/D configurations, including scan channels, input range, and polarities.

The A/D acquisition is initiated by a trigger signal. The data acquisition will start once the trigger signal matches the trigger conditions. Converted data are queued into the FIFO buffer, and then transferred to the host PC's memory for further processing.

Two acquisition modes: Software Polling and Programmable Scan are described in the following sections, including the timing, trigger modes, trigger sources, and transfer methods.

4.1.1 DAQ/DAQe/PXI-250x Series AD Data Format

The data format of the acquired 14-bit A/D data is 2’s Complement coding. Table 4-1 and 4-2 lists the valid input ranges and the ideal transfer characteristics.

Description	**Bipolar Analog Input Range**				**Digital code**
Full-scale Range	±10V	±5V	±2.5V	±1.25V	
Least significant bit	1120.78uV	610.39uV	305.19uV	152.60uV	
FSR-1LSB	9.998779V	4.999389V	2.499694V	1.249847V	1FFF
Midscale +1LSB	1120.78uV	610.39uV	305.19uV	152.60uV	0001
Midscale	0V	0V	0V	0V	0000
Midscale –1LSB	-1120.78uV	-610.39uV	-305.19uV	-152.60uV	3FFF
-FSR	-10V	-5V	-2.5V	-1.25V	2000

Table 4-1: Bipolar Input Range and Converted Digital Codes

Description	Unipolar Analog Input Range				Digital code
Full-scale Range	0V to 10V	0 to +5V	0 to +2.5V	0 to +1.25V	
Least significant bit	610.39uV	305.19uV	152.60uV	76.3uV	
FSR-1LSB	4.999389V	2.499694V	1.249847V	1.249923V	1FFF
Midscale +1LSB	5.000611V	2.500306V	1.250153V	0.625076V	0001
Midscale	5V	2.5V	1.25V	625mV	0000
Midscale –1LSB	4.999389V	2.499694V	1.249847V	1.249923V	3FFF
-FSR	0V	0V	0V	0V	2000

Table 4-2: Unipolar Input Range and Converted Digital Codes

4.1.2 Software Polling

This is the easiest way to acquire a single A/D data. The A/D converter performs one conversion whenever the dedicated software command is executed. The software would poll the conversion status and read the A/D data back when it is available.

This method is suitable for applications that need to acquire A/D data in real time. In this mode, the timing of the A/D conversion is fully controlled by software. However, it would be difficult to maintain a fixed A/D sampling rate.

4.1.3 Programmable Scan

This method is suitable for applications that need to acquire A/D data at a precise and fixed rate. A scan is a group of multiple channel samples and the scan interval is defined by the SI_counter. Likewise, the sample interval of the multiple channels is defined by the SI2_counter. Please refer to Table 4-4 for more information.

DAQ/DAQe/PXI-250x Series can sample multiple channels in continuous/discontinuous ascending sequence. For example, users may program DAQ/DAQe/PXI-250x Series to perform a scan in the channel sequence of 1-2-4-1-2-4…

There are 3 Trigger Modes available in Programmable Scan. They are Post-Trigger, Delay-Trigger, Post/Delay-Trigger with Retrigger.

Please refer to Table 4-3 for a brief summary on Trigger Modes and their Trigger Sources.

Trigger Mode	Description	Trigger Sources
Post-Trigger	Perform a scan right after the trigger occurs.	Software Trigger Digital Trigger Analog Trigger SSI AD Trigger
Delay-Trigger	Scan delayed by the amount of time programmed after the trigger	
Post/Delay-Trigger with Retrigger	Perform repeated scan while trigger occurs and it could be under Post-Trigger or De-lay-Trigger mode.	

Table 4-3: Trigger Modes and Corresponding Trigger Sources

4.1.4 Scan Timing and Procedure

There are 4 counters that need to be specified prior to programmable scans:

Counter Name	Width	Description	Notes
SI_counter	24-bit	**S**can **I**nterval, which defines the interval between each scan.	Scan Interval = SI_counter / Time-base*
SI2_counter	24-bit	**S**ampling **I**nterval, which defines the interval between each sampled channel.	Sampling Interval = SI2_counter / Timebase*
PSC_counter	24-bit	**P**ost **S**can **C**ounts, which defines how many scans to be performed with re-spect to each trigger.	
Delay_counter	16-bit	Define the delay time for scan after trigger.	Delay Time = (Delay_counter / Time-base*),Timebase*=40Mfor DAQ/DAQe/PXI-250x Series

Table 4-4: Summary of Counters for Programmable Scan

The relationship between counters and acquisition timing is illustrated in Figure 4-2.

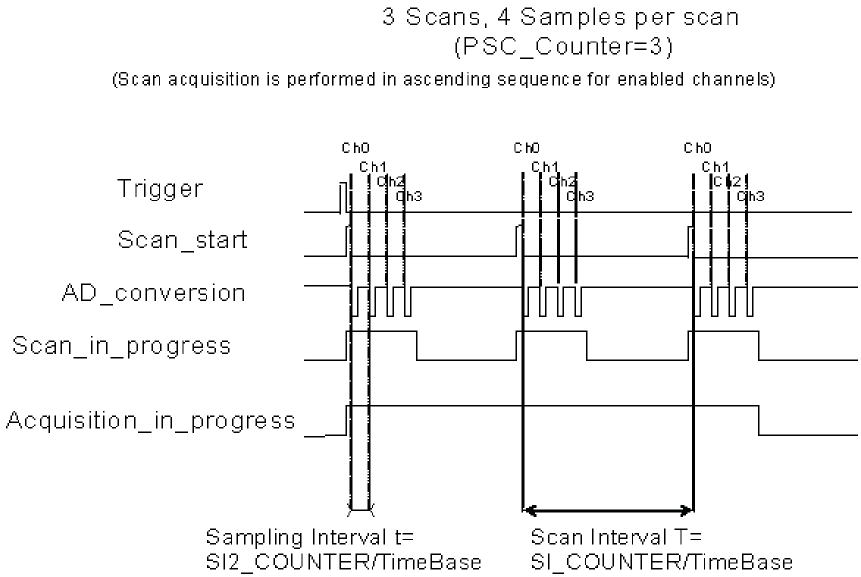


Figure 4-2: Timing for Scan

Note:

1. The maximum A/D sampling rate is 400KHz for DAQ/DAQe/PXI-250x Series therefore the minimum setting of SI2_counter is 100.
2. The Scan Interval can not be smaller than the interval of data Sampling Interval multiple by the Number of channels per Scan, i.e.: SI_counter >= SI2_counter * NumChan_Counter.

4.1.5 Trigger Modes

Post-Trigger Acquisition

Use post-trigger acquisition when users want to perform scans right after a trigger signal. The number of scans to be performed after the trigger signal is specified by the PSC_counter, as illustrated in Figure 4.3. The total acquired data length = (number_of_channels_enabled_for_scan_acquisition) * PSC_counter.

Delay Trigger Acquisition

Use delay trigger when users want to delay the scan after a trigger signal. The delay time is determined by the Delay_counter, as shown in Figure 4-4.

The counter counts down on the rising edges of Delay_counter clock source after the trigger signal. When the count reaches 0, DAQ/DAQE/PXI-250X SERIES starts to perform the scan. The acquired data length
= (number_of_channels_enabled_for_scan_acquisition) * PSC_counter. The Delay_counter clock source can be software selected from Internal 40MHz Timebase, external input (AFI-1), or General Purpose Timer/Counter Output 0/1.

Post-Trigger or Delay-trigger Acquisition with Retrigger

Use post-trigger or delay-trigger acquisition with retrigger when users want to perform repeated scans with respect to the repeated triggers. Figure 4-5 illustrates an example. Two scans are performed after the first trigger signal, and then wait for the next trigger signal. When the trigger signal occurs, it performs 2 more scans.

When retrigger function is disabled, only one trigger signal would be accepted after retrigger.

Note: Retrigger signals asserted during scan process will be ignored.

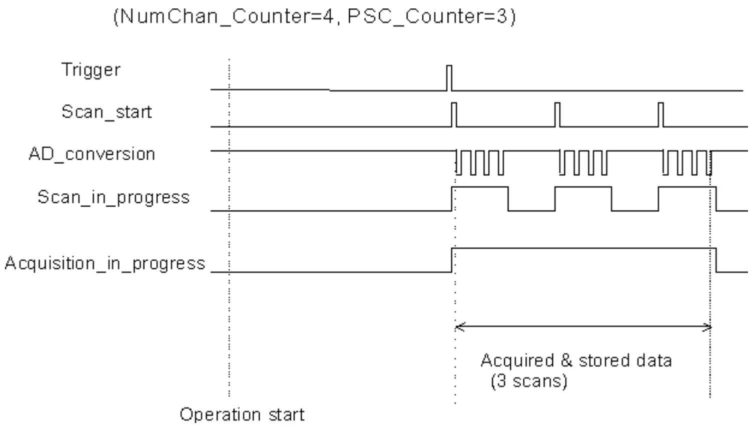


Figure 4-3: Post Trigger

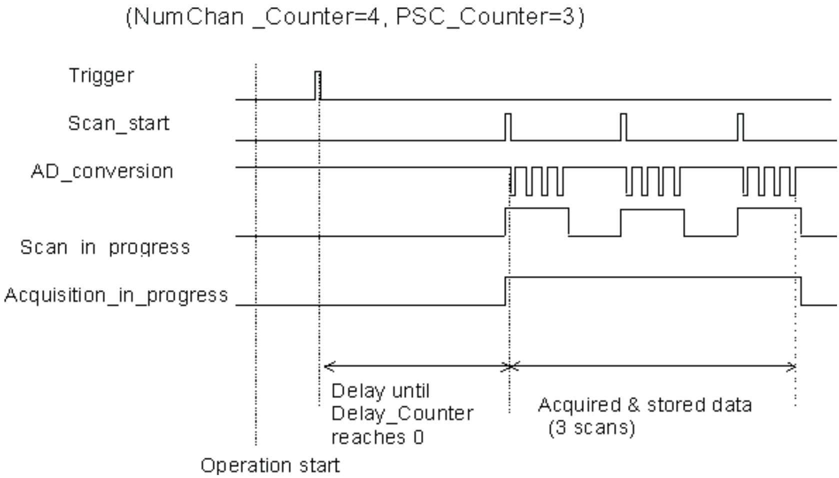


Figure 4-4: Delay Trigger

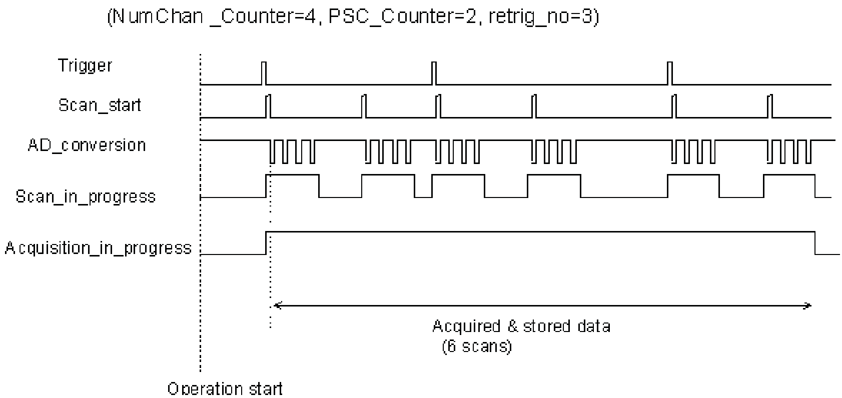


Figure 4-5: Post Trigger with Retrigger

4.1.6 Bus-mastering DMA Data Transfer

In programmable scan acquisition mode, all DAQ/DAQe/PXI series cards supports bus-mastering DMA data transfer. PCI bus-mastering DMA is necessary for high speed DAQ in order to utilize the maximum bus bandwidth. The bus-mastering controller controls the PCI bus when it becomes the master. Bus mastering reduces the size of the onboard memory and reduces CPU loading since data is directly transferred to the system memory with no host CPU intervention.

Bus-mastering DMA provides the fastest data transfer rate on a PCI bus. Once the analog input operation starts, control returns to your program. The hardware temporarily stores the acquired data in the onboard AD Data FIFO, then transfers the data to a user-defined DMA buffer memory in the computer. Note that even when the acquired data length is less than the Data FIFO, the AD data is not kept in the Data FIFO but rather directly transferred to the host memory by the bus-mastering DMA.

The DMA transfer mode is very complex to program. It is recommended that you use a high-level program library provided by the ADLINK driver to configure this card. By using a high-level programming library for high speed DMA data acquisition, you convert through their specified counters. After the AD trigger condition is matched, the data will be transferred to the system memory by the bus-mastering DMA.

The PCI controller also supports the scatter/gather bus mastering DMA function that enables transfer of large amounts of data by linking all the memory blocks into a continuous linked list.

In a multi-user or multitasking OS, like Windows or Linux, it is difficult to allocate a large continuous memory block to do the DMA transfer. Therefore, the PCI controller provides the function of scatter-gather or chaining mode DMA to link the non-continuous memory blocks into a linked list, allowing transfers of very large amounts of data without being limited by the fragment of small size memory. You may configure the linked list for the input DMA channel or the output DMA channel. Figure 4-6 shows a linked list that is constructed by three DMA descriptors. Each descriptor contains a PCI address, a PCI dual-address, a transfer size, and the pointer to the next descriptor. PCI address and PCI dual address cycle support 64-bit addresses which can be mapped into more than 4 GB of the address space. You can allocate many small size memory blocks and chain their associative DMA descriptors altogether by their application programs.

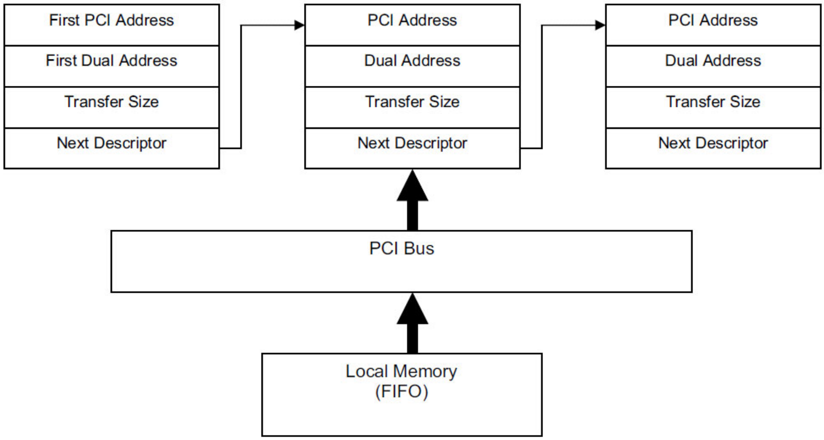


Figure 4-6: Linked List of PCI Address DMA Descriptors

In non-chaining mode, the maximum DMA data transfer size is 2M double words (8 MB). However, by using chaining mode-scatter/ gather, there is no limitation for the DMA data transfer size. You may also link the descriptor nodes circularly to achieve a multi-buffered mode DMA.

4.2 D/A Conversion

DAQ/DAQe/PXI-250x Series offers flexible and versatile analog output scheme to fit users' complex field applications. In order to take full advantages of DAQ/DAQe/PXI-250x Series, we suggest users carefully read the following con-tents.

Architecture

There are up to 8-channel of 12-bit Digital-to-Analog Converter (DAC) available in the DAQ/DAQe/PXI-2502. Four D/A channels are packed into one D/A group, i.e., DAQ/DAQe/PXI-2502 contains two D/ A groups, and DAQ/DAQe/PXI-2501 has only one D/ A group.

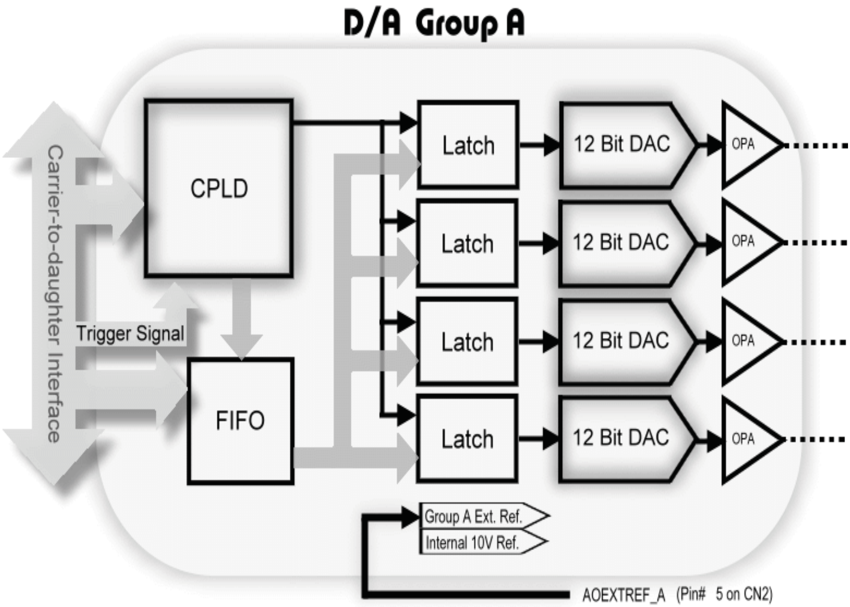


Figure 4-7: Block Diagram of D/A Group

(Group B of DAQ/DAQE/PXI-2502 is identical to Group A shown above)

Figure 4-7 shows the D/A block diagram. DAC are controlled implicitly by CPLD and have their outputs updated only when digital codes for all enabled DA channels are ready and latched. This ensures D/A conversions to be synchronized for each channel in the same D/A group. Users can utilize this property to perform multi-channel waveform generation without any phase-lag.

Hardware controlled Waveform Generation

FIFO is a hardware first-in first-out data queue, which holds temporary digital codes for D/A conversion. When DAQ/DAQe/PXI-250x Series operates in Waveform Generation mode, the waveform patterns are stored in FIFO, with 8K maximum samples. Waveform patterns larger than 8K are also supported by utilizing bus-mastering DMA transfer supported by PCI controller. Data format in FIFO is shown in Figure 4-8.

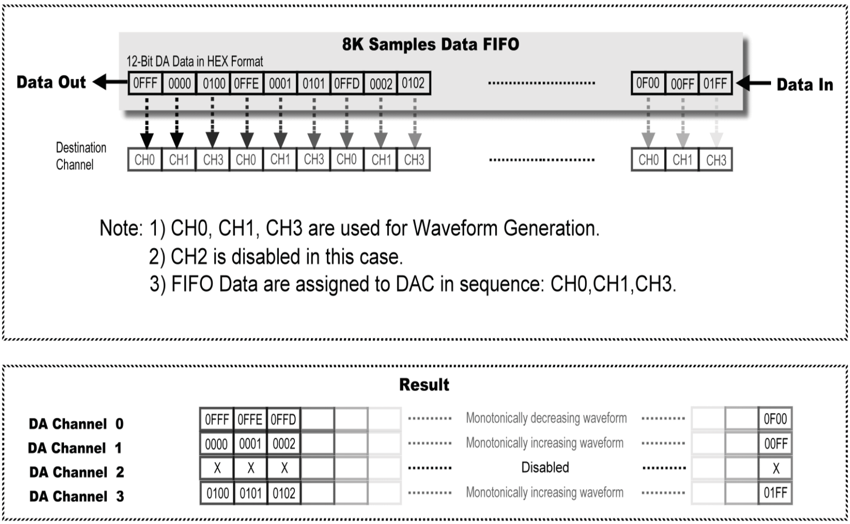


Figure 4-8: Data Format in FIFO and Mapping

With hardware-based Waveform Generation, D/A conversions are updated automatically by CPLD rather than application software. Unlike the conventional Software-based Waveform Generation, the precise hardware timing control guarantees non-distorted waveform generation even when host CPU is under heavy loading. Detailed function setup will be explained in Section 4.2.2.

NOTE: When using waveform generation mode, all the four DACs in the same D/A group must be configured for the same mode. However, any one of the DAC can be disabled. If users need to use the software update mode, they can use another D/A group on the DAQ/DAQe/PXI-2502.

Setting up the DACs

Before using the DACs, users should setup the reference source and its polarity. Each DAC has its own reference and polarity settings. For example; the internal voltage reference of D/A Group A is tied to internal +10V, however, users can still connect external reference thru AOEXTREF (pin 5 on CN2), for example to a +3.3V voltage source. Therefore, each DAC in D/ A Group A has two reference options: 10V or 3.3V. However, DA update timing, trigger Source, and trigger/stop mode are all the same throughout that D/ A Group.

DAQ/DAQe/PXI-250x Series provides the capability to fine tune the voltage reference from the external source. The external reference is fed thru an on board calibrated circuit, with programmable offset. Users can utilize this capability to generate precise D/A outputs.

NOTE: The range of external voltage reference should be within ±10V.

Utilizing Multiplying Characteristic of DACs

The D/A reference selection let users fully utilize the multiplying characteristics of the DACs. Digital codes sent to the D/A converters will be multiplied by the reference to generate output.

Magnitude	Bipolar	Unipolar	
	Output	Output	Digital Code
FSR – LSB	+Vref * (2046 / 2048)	Vref * (4095 / 4096)	0FFF
Midscale + LSB	+Vref * (1 / 2048)	Vref * (2049 4096)	0801
Midscale	0	Vref * (2048 / 4096)	0800
Midscale – LSB	-Vref * (1 / 2048)	Vref * (2047 / 4096)	07FF
FSR + LSB	-Vref * (2046 / 2048)	Vref * (1 / 4096)	0001
-FSR	-Vref	0	0000

Table 4-5: D/A Output Versus Digital Codes

The DAQ/DAQe/PXI-250x Series can generate standard and arbitrary functions, continuously or piece-wise. Appendix A demonstrates possible wave-form patterns generated by the DAQ/DAQe/PXI-250x Series in combination with various counters, clock sources, and voltage references.

Software Update

This method is suitable for applications that need to generate D/A output controlled by user programs. In this mode, the D/A converter generates one output once the software command is issued. However, it would be difficult to determine the software update rate under a multi-task OS like Windows.

Waveform Generation

This method is suitable for applications that need to generate waveforms at a precise and fixed rate. Various programmable counters will facilitate users to generate complex waveforms with great flexibility.

There are three event signals involved in Waveform Generation: Start, DAWR (DA WRite), and Stop. Please refer to Table 4.2.2 for a brief summary on Waveform Generation Events and their corresponding Trigger Sources.

For more information on Trigger Mode, Stop Mode, Time-base, and Trigger Sources, please refer to sections 4.2, 4.1, and 4.5, respectively.

Signal	Descriptions	Valid Sources
Start	Start Waveform Generation process.	Software Trigger Ext. Digital Trigger Analog Trigger SSI Trigger
DAWR	Write data to the DAC on the fal-ling edges of DAWR.	Internal Update External Update SSI Update
Stop	Stop Waveform Generation	Software Trigger Ext. Digital Trigger Analog Trigger

Table 4-6: Trigger Signals and Corresponding Signal Sources

Waveform Generation Timing

Six counters interact with the waveform to generate different DAWR timing, thus forming different waveforms. They are described in Table 4-7.

Counter Name	Width	Description	Note
UI_counter	24-bit	Update Interval, which defines the update interval between each data output.	Update Interval = UI_counter / Time-base*.
UC_counter	24-bit	Update Counts, which defines the number of data in a waveform.	When value in UC_counter is smaller than the size of waveform patterns, the waveform is generated piece-wisely.
IC_counter	16-bit	Iteration Counts, which defines how many times the waveform is generated.	

Table 4-7: Summary of Counters for Waveform Generation

DLY1_counter	16-bit	Define the delay time for waveform generation after the trigger signal.	Delay Time = (DLY1_counter / Clock Timebase)
DLY2_counter	16-bit	Define the delay time to separate consecutive waveform generation. Effective only in Iterative Waveform Generation mode.	Delay Time = (DLY2_counter / Clock Timebase)
Trig_counter	16-bit	Define the acceptable start trigger count when re-trigger function is enabled	Timebase*= 40M for DAQ/ DAQe/PXI-250x Series

Table 4-7: Summary of Counters for Waveform Generation

NOTE:

The maximum D/A update rate is 1MHz. Therefore the minimum setting of UI_counter is 40.

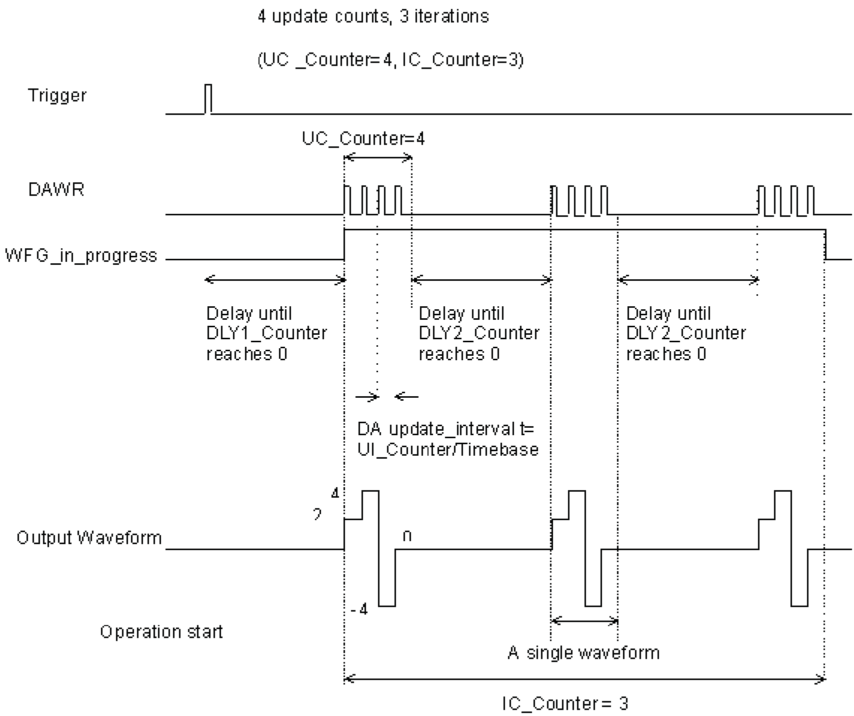


Figure 4-9: Typical D/A timing of waveform generation

(Assuming the data in the data buffer are 2V, 4V, -4V, 0V)

Trigger Modes

Post-Trigger Generation

Use post-trigger generation when users want to generate waveform right after a trigger signal. The number of patterns to be updated after the trigger signal is specified by UC_counter* IC_counter, as illustrated in Figure 4-9

Delay-Trigger Generation

Use delay-trigger when users want to delay the waveform generation after the trigger signal. The delay time is determined by DLY1_counter, as shown in Figure 4-10.

The counter counts down on the rising edges of DLY1_counter clock source after the start trigger signal. When the count reaches zero, DAQ/DAQe/PXI-250x Series starts to generate the waveform. The DLY1_counter clock source can be software selected from the Internal 40MHz Timebase, external clock input (AFI-0), or GPTC output 0/1.

Post-Trigger or Delay-Trigger with Retrigger

Use post-trigger or delay-trigger with retrigger when users want to generate multiple waveforms with respect to multiple incoming trigger signals. Users can set Trig_counter to specify the number of acceptable trigger signals.

Figure 4-11 illustrates an example. Two waveforms are generated after the first trigger signal (Iterative Waveform Generation is used in this example, please refer to Section 4.2 for details). The board then waits for another trigger signal. When the next trigger signal is asserted, the board generates two more waveforms. After three trigger signals, as specified in Trig_Counter, no more triggers signals will be accepted unless software trig- ger reset command is executed.

NOTE: Start Trigger signals asserted during waveform generation process will be ignored.

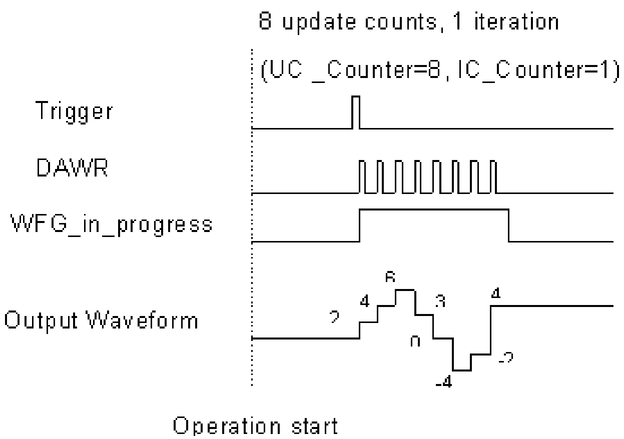


Figure 4-10: Post-Trigger Generation

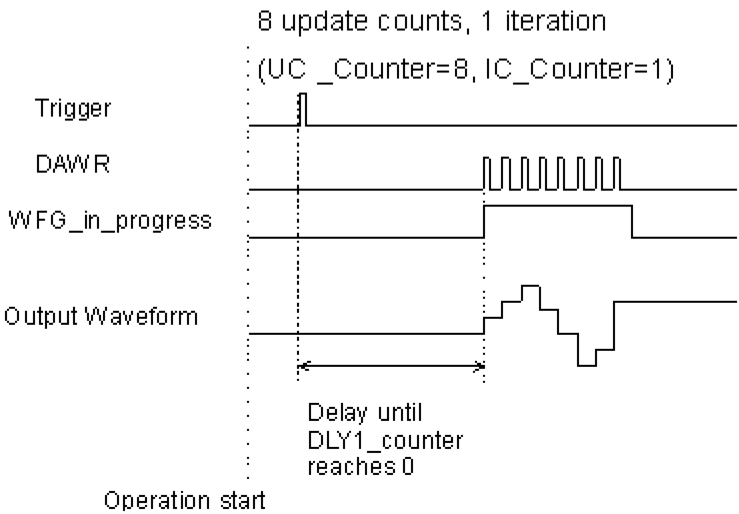


Figure 4-11: Delay-Trigger Generation

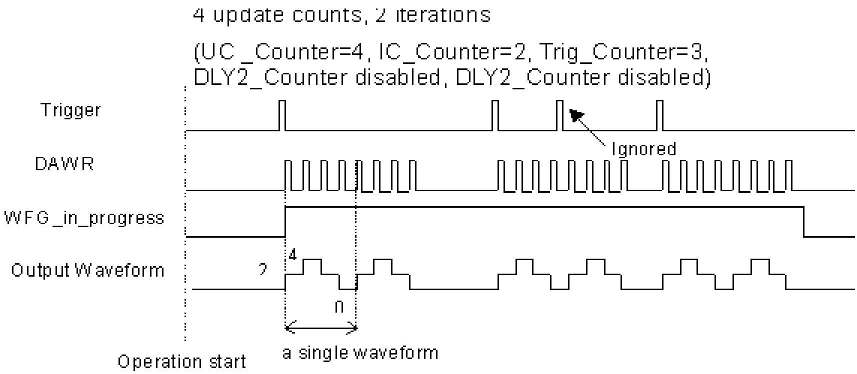


Figure 4-12: Post-Trigger with Retrigger Generation

Iterative Waveform Generation

Users can set IC_counter to generate iterative waveforms, no matter which Trigger Mode is used. The IC_counter stores the iteration number. Examples are shown in Figure 4-13 and 4-14.

When IC_counter is disabled, the waveform generation will not stop until a stop trigger is asserted. For Stop Mode, please refer to Section 4.2 for details.

An on-board data FIFO is used to buffer the waveform patterns for waveform generation. If the size of a single waveform is smaller than that of the FIFO, after initially loading the data from the host PC's memory, the data in FIFO will be re-used when a single waveform generation is completed. In other words, it won't occupy the PCI bandwidth afterwards. How- ever, if the size of a single waveform were larger than that of the FIFO, it needs to be intermittently loaded from the host PC's memory via DMA, thus PCI bandwidth would be occupied.

If the value specified in UC_counter is smaller than the sample size of the waveform patterns, the waveform will be generated piece-wisely. For example, if users defined a 16-sample sine wave and set the UC_counter to 2, the generated waveform will be a 1/8-cycle sine wave for every waveform period. In other words, a complete sine wave will be generated for every 8-iterations. If value specified in UC_counter is larger than the sample size of waveform LUT, say, 32; the generated waveform will be a 2-cycle sine wave for every waveform period.

In conjunction with different trigger modes and counter setups, users can manipulate a single waveform to generate different, more complex waveforms. For more information, please refer to Appendix A.

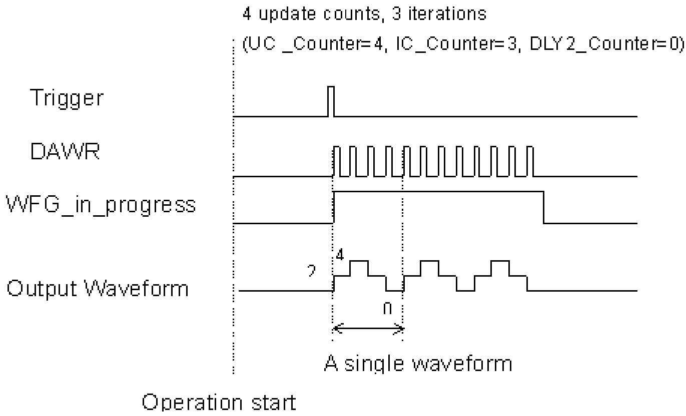


Figure 4-13: Finite iterative waveform generation w/Post-trigger

(Assuming the digital codes in the FIFO are 2V, 4V, 2V, 0V)

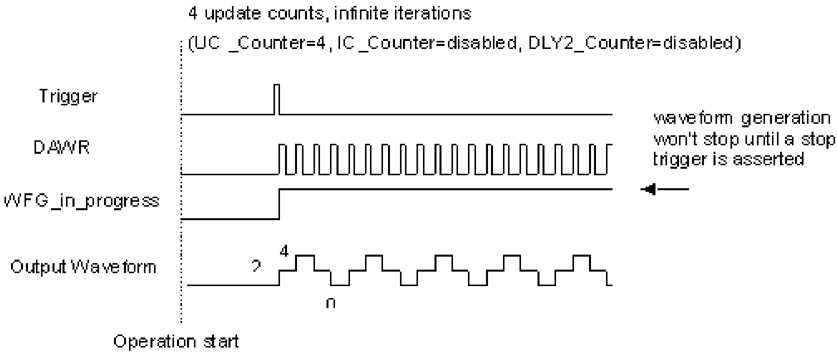


Figure 4-14: Infinite iterative waveform generation w/Post-trigger

(Assuming the digital codes in the FIFO are 2V, 4V, 2V, 0V)

DLY2_Counter in iterative Waveform Generation

To expand the flexibility of Iterative Waveform Generation, DLY2_counter was implemented to separate consecutive waveform generations.

The DLY2_counter starts counting down right after a single waveform generation is completed. When it reaches zero, the next iteration of waveform generation will start as shown in Figure 4.2.3. If users are generating waveform piece-wisely, the next piece of waveform will be generated. The DLY2_counter clock source can be software selected from Internal 40MHz Timebase, external clock input (AFI-0), or GPTC output 0/1.

Stop Modes

Users can stop waveform generation while it is still in progress, either by hardware or software trigger. The stop trigger sources can be software selected from Internal software trigger, external digital trigger (AFI-0/1), or analog trigger. Three stop modes are provided to stop finite or infinite waveform generation.

Stop Mode I

After a mode I stop trigger is asserted, the waveform generation stops immediately. Figure 4-15 illustrates an example.

Stop Mode II

After a mode II stop trigger is asserted, the waveform generation continues to generate a complete waveform then stops the operation. Take Figure 4-16 as an example. Since UC_counter is set to 4, the total generated data points must be a multiple of 4.

Users can check WFG_in_progress (waveform generation in progress) status by software read-back to confirm the stop of a waveform generation.

Stop Mode III

After a mode III stop trigger is asserted, the waveform generation continues until the iterative number of waveforms specified in IC_Counter is completed. Take Figure 4-17 for example. Since IC_Counter is set to 3, the total generated waveforms must be a multiple of 3.

Users can check WFG_in_progress (waveform generation in progress) status by software read-back to confirm the stop of a waveform generation.

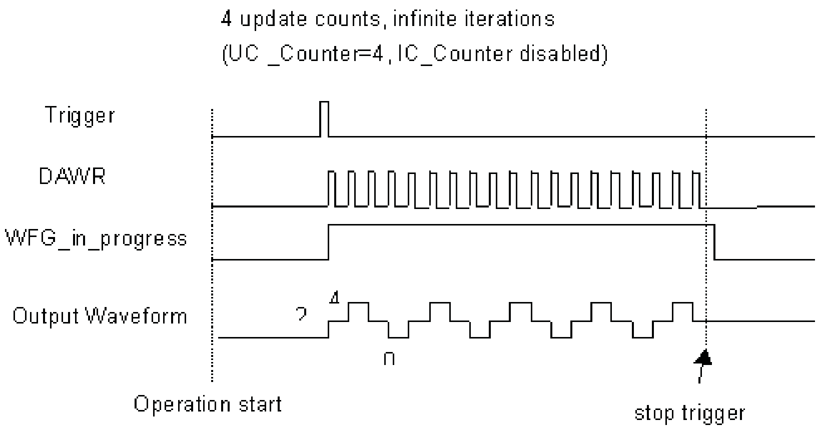


Figure 4-15: Stop mode I

(Assuming the data in the data buffer are 2V, 4V, 2V, 0V)

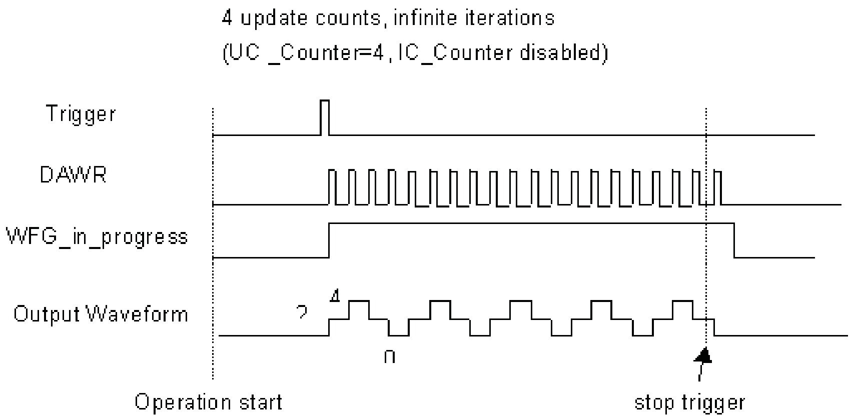


Figure 4-16: Stop mode II

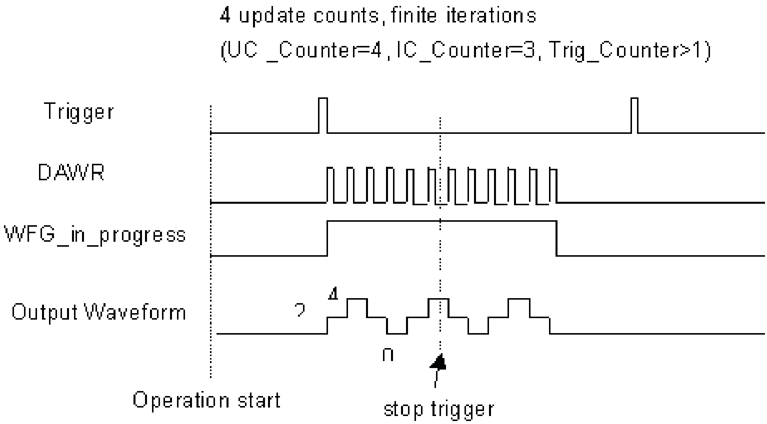


Figure 4-17: Stop mode III

4.3 General Purpose Digital I/O

DAQ/DAQE/PXI-250x Series provides 24-line general-purpose digital I/ O (GPIO) through a 82C55A chip.

The 24-line GPIO are separated into three ports: Port A, Port B and Port C. High nibble (bit[7…4]), and low nibble (bit[3…0]) of each port can be individually programmed to be either inputs or outputs. Upon system startup or reset, all the GPIO pins are reset to high impedance inputs.

For more information on programmable I/O chip 82C55A, please refer to http://www.intel.com.

4.4 General Purpose Timer/Counter Operation

Two independent 16-bit up/down timer/counter are embedded in FPGA firmware for users applications. They have the following features:

- Direction of counting can be controlled via hardware or software.
- Selectable counter clock source from either internal or external clock up to 10MHz.
- Programmable gate selection.
- Programmable input and output signal polarities, either active-high or active-low.
- Initial Count can be loaded via software
- Current count value can be read-back by software without affecting circuit operation

4.4.1 Timer/Counter functions basics

Each timer/counter has three inputs that can be controlled via hardware or software. They are clock input (GPTC_CLK), gate input (GPTC_GATE), and up/down control input (GPTC_UPDOWN).

The GPTC_CLK input acts as a clock source to the timer/counter. Active edges on the GPTC_CLK input increment or decrement the counter. The GPTC_UPDOWN input determines whether the counter's counting-up or counting-down. The GPTC_GATE input is a control line, which acts as a counter enable or a counter trigger signal in different modes.

The output of timer/counter is GPTC_OUT. After power-up, GPTC_OUT is pulled high by a 10K resistor. GPTC_OUT goes low after the DAQ board is initialized.

All the polarities of input/output signals can be programmed via software. In this chapter, all timing figures assume that GPTC_CLK, GPTC_GATE, and GPTC_OUT are set to be positive-logic. (i.e. they're triggered on the rising-edge)

4.4.2 General Purpose Timer/Counter modes

Eight programmable timer/counter modes are provided. All modes start operations following the software start command. The GPTC software reset command initializes the status of the counter and re-loads the initial value to the counter.

Mode 1: Simple Gated-Event Counting

In this mode, the counter counts the number of pulses on the GPTC_CLK after the software start. Initial count value can be loaded via software. Current count value can be read-back by software at any time. GPTC_GATE is used to enable/disable counting. When GPTC_GATE is inactive, the counter halts the current count value. Figure 4-18 illustrates the operation with initial count = 5 in down-counting mode.

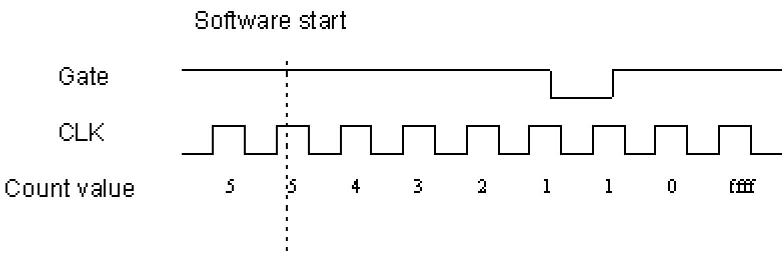


Figure 4-18: Mode 1 Operation

Mode 2: Single Period Measurement

In this mode, the counter counts the period of the signal on GPTC_GATE in terms of GPTC_CLK. Initial count can be loaded via software. After the software start, the counter counts the number of active edges on GPTC_CLK between two active edges of GPTC_GATE. After the completion of the period measurement, GPTC_OUT outputs high and current count value can be read-back by software. Figure 4-19 illustrates the operation where initial count = 0, up-counting mode.

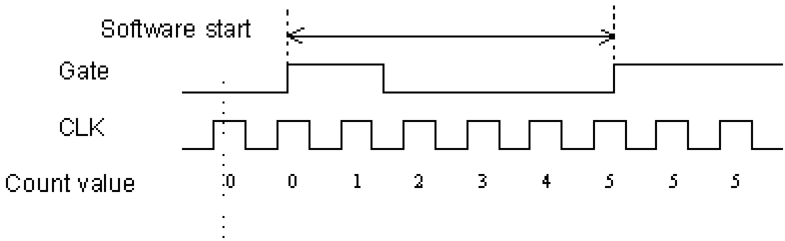


Figure 4-19: Mode 2 Operation

Mode 3: Single Pulse-width Measurement

In this mode, the counter counts the pulse-width of the signal on GPTC_GATE in terms of GPTC_CLK. Initial count can be loaded via software. After the software start, the counter counts the number of active edges on GPTC_CLK when GPTC_GATE is active. GPTC_OUT outputs high, and current count value can be read-back via software after the completion of the pulse-width measurement. Figure 4-20 illustrates the operation where initial count = 0 in up-counting mode.

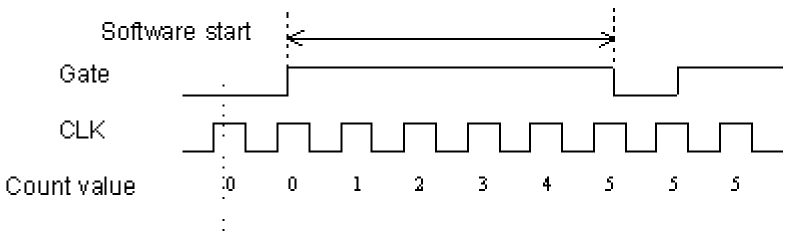


Figure 4-20: Mode 3 Operation

Mode 4: Single Gated Pulse Generation

This mode generates a single pulse with programmable delay and programmable pulse-width following the software start. These software programmable parameters could be specified in terms of periods of the GPTC_CLK. GPTC_GATE is used to enable/disable counting. When GPTC_GATE is inactive, the counter halts the counting. Figure 4-20 il-lustrates the generation of a single pulse with pulse-delay of two and pulse-width of four

.

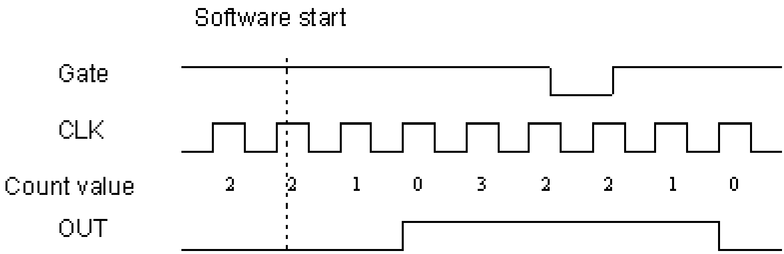


Figure 4-21: Mode 4 Operation

Mode 5: Single Triggered Pulse Generation

This function generates a single pulse with programmable delay and programmable pulse-width following an active GPTC_GATE edge. These software programmable parameters can be specified in terms of periods of the GPTC_CLK input. Once the first GPTC_GATE edge triggers the single pulse, GPTC_GATE takes no effect until the software start is re-executed. Figure 4-22 illustrates the generation of a single pulse with pulse delay of two and pulse-width of four.

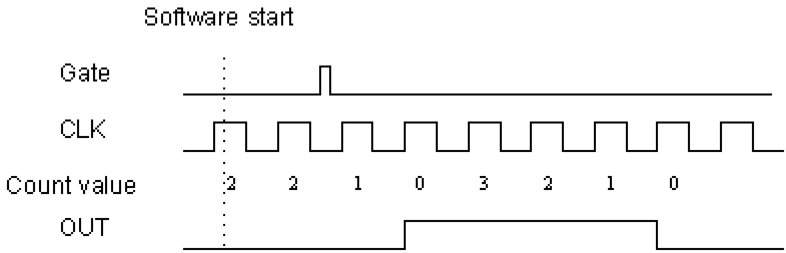


Figure 4-22: Mode 5 Operation

Mode 6: Re-triggered Single Pulse Generation

This mode is similar to mode 5 except that the counter generates a pulse following every active edge on GPTC_GATE. After the software start, every active GPTC_GATE edge triggers a single pulse with programmable delay and pulse-width. Any GPTC_GATE trigger that occurs during the pulse generation would be ignored. Figure 4-23 illustrates the generation of two pulses with pulse delay of two and pulse-width of four.

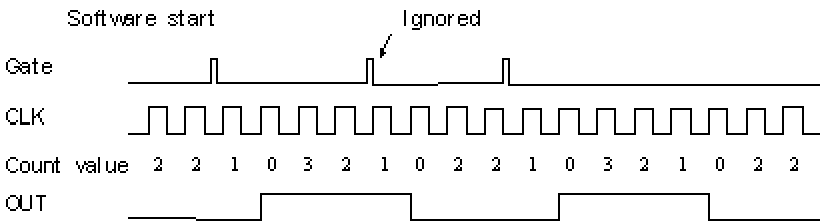


Figure 4-23: Mode 6 Operation

Mode 7: Single Triggered Continuous Pulse Generation

This mode is similar to mode 5, except that the counter generates continuous periodic pulses with programmable pulse interval and pulse-width following the first active edge of GPTC_GATE. Once the first GPTC_GATE edge triggers the counter, GPTC_GATE takes no effect until the software start is re-executed. Figure 4-24 illustrates the generation of two pulses with pulse delay of four and pulse-width of three.

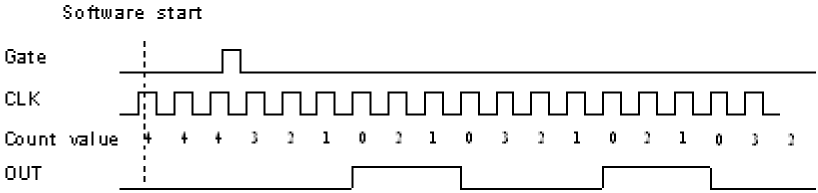


Figure 4-24: Mode 7 Operation

Mode 8: Continuous Gated Pulse Generation

This mode generates periodic pulses with programmable pulse interval and pulse-width following the software start. GPTC_GATE is used to enable/disable counting. When GPTC_GATE is inactive, the counter halts the current count value. Figure 4-25 illustrates the generation of two pulses with pulse delay of four and pulse-width of three

.

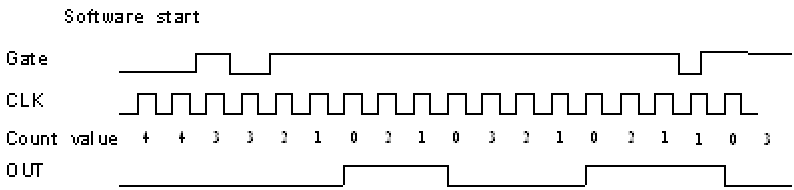


Figure 4-25: Mode 8 Operation

4.5 Trigger Sources

We provide flexible trigger selections in DAQ/DAQE/PXI-250x Series. In addition to software trigger, DAQ/DAQE/PXI-250x Series also supports external analog and digital triggers. Users can configure the trigger source for A/D and D/A processes individually via software. Note that the A/D and the D/A conversion share the same analog trigger.

4.5.1 Software-Trigger

This trigger mode does not need any external trigger source. The trigger asserts right after users execute the specified function call. A/D and D/A processes can receive an individual software trigger.

4.5.2 External Analog Trigger

The analog trigger circuitry routing is shown in the Figure 4.5.1. The analog multiplexer selects either a direct analog input from the EXTATRIG pin (SRC1 in Figure 4-25) on the 68-pin connector CN1 or the input signal of ADC (SRC2 in Figure 4-25). The range of trigger level for SRC1 is ±10V and the resolution is 78mV (please refer to Table 4-8), while the trigger range of SRC2 is the full-scale range of AD input, and the resolution is the desired range divided by 256.

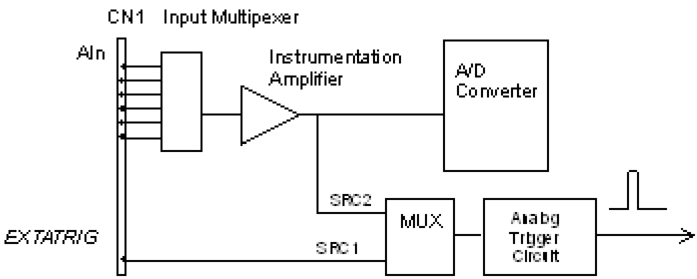


Figure 4-26: Analog trigger block diagram

Trigger Level digital setting	Trigger voltage
0xFF	9.92V
0xFE	9.84V
---	---
0x81	0.08V
0x80	0
0x7F	-0.08V
---	---
0x01	-9.92V
0x00	-10V

Table 4-8: Analog trigger SRC1 (EXTATRIG) ideal transfer characteristic

The trigger signal asserts when an analog trigger condition is meet. There are five analog trigger conditions in DAQ/DAQE/PXI-250x Series. DAQ/DAQE/PXI-250x Series uses 2 threshold voltages: Low_Threshold and High_Threshold to compose 5 different trigger conditions. Users can con-figure the trigger conditions easily via software.

Below-Low analog trigger condition

Figure 4-27 shows the below-low analog trigger condition, the trigger signal asserts when the input analog signal is lower than the Low_Threshold voltage. High_Threshold setting is not used in this trigger condition.

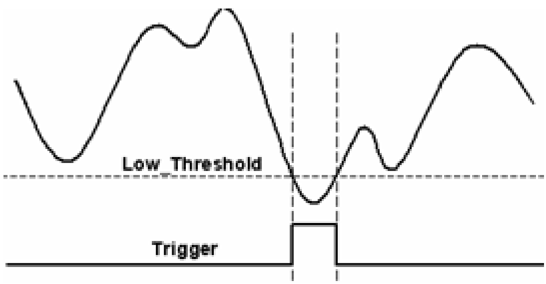


Figure 4-27: Below-Low analog trigger condition

Above-High analog trigger condition

Figure 4-28 shows the above-high analog trigger condition, the trigger signal asserts when the input analog signal is higher than the High_Threshold voltage. The Low_Threshold setting is not used in this trigger condition.

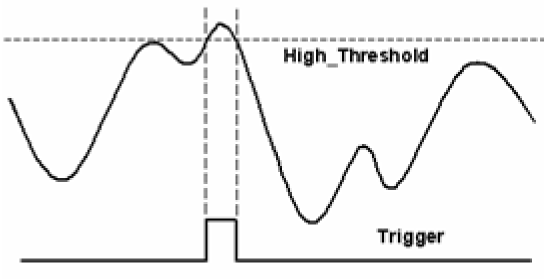


Figure 4-28: Above-High analog trigger condition

Figure 4-29 shows the inside-region analog trigger condition, the trigger signal asserts when the input analog signal level falls in the range between the High_Threshold and the Low_Threshold voltages.

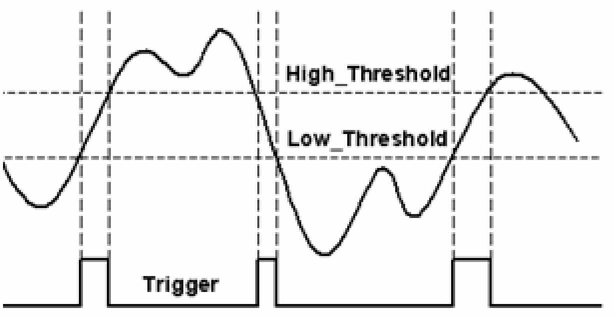


Figure 4-29: Inside-Region analog trigger condition

High-Hysteresis analog trigger condition

Figure 4-30 shows the high-hysteresis analog trigger condition, the trigger signal asserts when the input analog signal level is higher than the High_Threshold voltage, where the hysteresis region is determined by the Low_Threshold voltage.

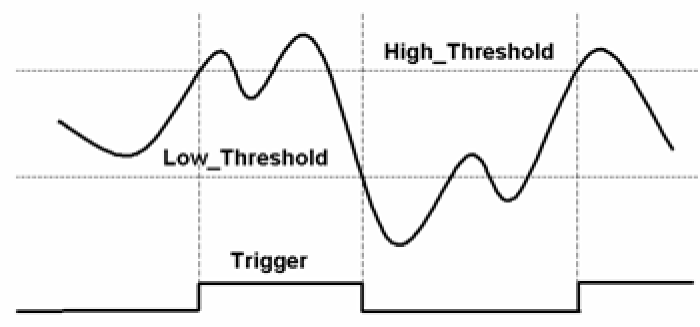


Figure 4-30: High-Hysteresis analog trigger condition

Low-Hysteresis analog trigger condition

Figure 4-30 shows the low-hysteresis analog trigger condition, the trigger signal asserts when the input analog signal level is lower than the Low_Threshold voltage, where the hysteresis region is determined by the High_Threshold voltage.

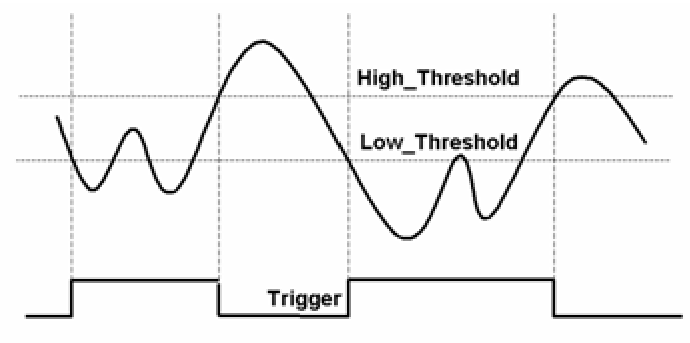


Figure 4-31: Low-Hysteresis analog trigger condition

4.6 Timing Signals

In order to meet the requirements for user-specific timing or synchronizing multiple boards, DAQ/DAQE/PXI-250x Series provides a flexible interface for connecting timing signals with external circuitry or other boards. The DAQ timing of the DAQ/DAQE/PXI-250x Series is composed of a bunch of counters and trigger signals in the FPGA on board.

There are 7 timing signals related to the DAQ timing, which in turn influence the A/D, D/A process, and GPTC operation. These signals are fed through the Auxiliary Function Inputs pins (AFI) or the System Synchronization Interface bus (SSI). We implemented a multiplexer in the FPGA to select the desired timing signal from these inputs, as shown in the Figure 4-32.

Users can use the SSI to achieve synchronization between multiple boards, or use the AFI to derive timing signals from an external timing circuit.

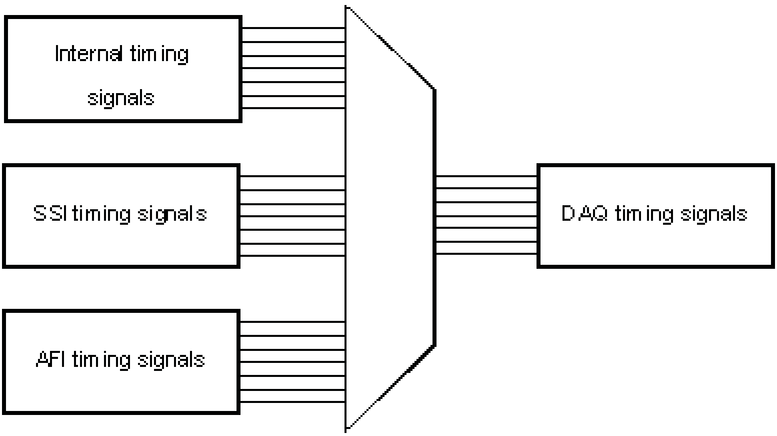


Figure 4-32: DAQ signals routing

4.6.1 System Synchronization Interface

SSI uses bi-directional I/O to provide flexible connections between boards. You can choose each of the 7 timing signals and which board to be the SSI master. The SSI master can drive the timing signals of the slaves. Users can thus achieve better synchronization between boards.

Note that when power-up or reset, the DAQ board is reset to using its internal timing signals.

5 Calibration

This chapter introduces the calibration process to minimize AD measurement errors and DA output errors.

DAQ/DAQE/PXI-250x Series is factory calibrated before shipment. The onboard high precision band-gap voltage reference together with TrimDAC compensates for unwanted offsets and gain errors, caused by environment variation or component aging.

5.1 Auto-calibration

The auto-calibration feature of DAQ/DAQE/PXI-250x Series facilitates users completing a calibration process, without the necessities for any external voltage references or measurement devices.

The onboard auto-calibration circuitry is composed of a precision band-gap voltage reference, an ADC and a TrimDAC. TrimDAC is a multi-channel DAC that generates DC offsets that counteract the offsets from the main DACs. Digital codes for the TrimDAC, as well as the temperature and the date of the calibration, are stored in the onboard EEPROM. We do not recommend end-users to adjust the onboard band-gap voltage reference in anyway, unless an ultra-precision calibrator is available.

Due to temperature, humidity variations, and component aging, the precision of DAQ board may degrade over time. It is suggested that users periodically calibrate the DAQ board. The user calibration constants can also be stored in the onboard EEPROM.

Note:

1. Before auto-calibration procedure starts, it is recommended to warn up the card for at least 15 minutes.
2. Please remove the cable before an auto-calibration procedure is initiated because the DA outputs would be changed in the process of calibration.

5.2 Saving Calibration Constants

An onboard EEPROM is used to store calibration constants. In addition to a default bank that stores factory calibration constants, there are three user banks. Users can save the subsequently performed calibration constants in anyone of these user banks. ADLINK provides software for users to save calibration constants in an easy manner.

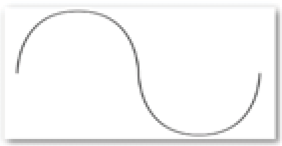
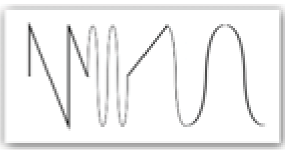
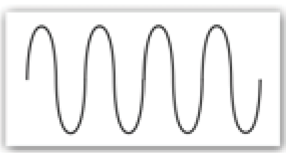
5.3 Loading Calibration Constants

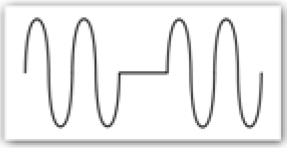
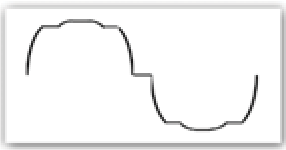
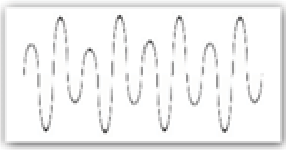
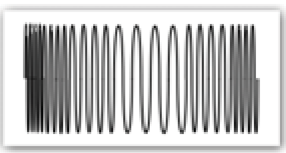
Users can calibrate DAQ board in three sites and store the calibration constants into different user banks. When moving DAQ board from one site to another, users can load the calibration constants without re-calibration. ADLINK provides software for users to load calibration constants in an easy manner.

Appendix A Waveform Generation Demonstration

Combined with 6 counters, selectable trigger sources, external reference sources, and time base, DAQ/DAQE/PXI-250x Series provides the capabilities to generate complex waveforms. Various modes shown below can be mixed together to generate waveforms that are even more complex.

Although users can always load a new waveform to generate any desired waveform, we suggest using hardware capabilities to maximize both efficiency and flexibility.

Standard Function	
	Waveforms including sine wave, triangular wave, saw wave, ramp, etc., can be converted to Waveform LUT. Using larger waveform means trading maxi-mum output rate for lower harmonic distortion.
Arbitrary Function	
	User defined arbitrary function without size limit can be generated. Users can also concatenate various standard functions of same length into one arbitrary function and setup piece-wise generation, so each standard function can be generated in sequence, with a user definable intermediate space.
Standard Function w. Frequency Variant	
	Users can alter the frequency of generated waveforms by driving DAWR from external signal via AF0/AF1/SSI. The resultant updating rate should be kept within1MHz. In this demo, iterative generation is used.

Iterative Generation w. Intermediate Space	
	Utilize DLY2_counter to separate consecutive waveform generations in iterative generation mode. In this demo, the original standard sine wave is repeated several times as specified in IC_counter, with intermediate space determined by DLY2_counter.
Piece-wise Generation	
	When the value specified in UC_counter is smaller than the sample size of waveform, the waveform is generated piece-wisely. The intermediate space between each piece is determined by DLY2_counter. In this demo, the UC_counter is set to 1/8 of the sample size of waveform.
Amplitude Modulated	
	When external D/A reference is used, applying sinusoidal voltage reference will result in an amplitude modulated (AM) waveform generation. Users can use one D/A channel to generate sine wave, loop it back to AOEXTREF_A/ B pin, and generate AM waveform by another D/A channel using external reference. All can be done in a single D/A group.
Frequency Modulated	
	By feeding AFI0/AFI1 with PWM source, pulse train from VCO, or any time-varying digital signal, DAQ/DAQE/PXI-250x Series is capable of generating frequency modulated (FM) waveform. Since all four channels are synchronized in a D/A group, precise quadrature waveform generation is guaranteed, provided the waveform are shifted 90-degree for the other channel. Phase difference of any degree can also be setup. Combined with external High-speed programmable Digital I/O card, Phase-Shift-Keying or Phase-Reversal-Keying can also be achieved.

Important Safety Instructions

For user safety, please read and follow all instructions, Warnings, Cautions, and Notes marked in this manual and on the associated device before handling/operating the device, to avoid injury or damage.

S'il vous plaît prêter attention stricte à tous les avertissements et mises en garde figurant sur l'appareil , pour éviter des blessures ou des dommages.

- Read these safety instructions carefully.
- Keep the User's Manual for future reference.
- Read the Specifications section of this manual for detailed information on the recommended operating environment.
- The device can be operated at an ambient temperature of 50ºC.
- When installing/mounting or uninstalling/removing device, or when removal of a chassis cover is required for user servicing:
  - Turn off power and unplug any power cords/cables.
  - Reinstall all chassis covers before restoring power.
- To avoid electrical shock and/or damage to device:
  - Keep device away from water or liquid sources.
  - Keep device away from high heat or humidity.
  - Keep device properly ventilated (do not block or cover ventilation openings).
  - Always use recommended voltage and power source settings.
  - Always install and operate device near an easily accessible electrical outlet.
  - Secure the power cord (do not place any object on/over the power cord).
  - Only install/attach and operate device on stable surfaces and/or recommended mountings.
- If the device will not be used for long periods of time, turn off and unplug it from its power source
- Never attempt to repair the device, which should only be serviced by qualified technical personnel using suitable tools
- A Lithium-type battery may be provided for uninterrupted backup or emergency power.

CAUTION:

Risk of explosion if battery is replaced with one of an incorrect type; please dispose of used batteries appropriately.
Risque d'explosion si la pile est remplacée par une autre de type incorrect. Veuillez jeter les piles usagées de façon appropriée.

- The device must be serviced by authorized technicians when:
  - The power cord or plug is damaged.
  - Liquid has entered the device interior.
  - The device has been exposed to high humidity and/or moisture.
  - The device is not functioning or does not function according to the User's Manual.
  - The device has been dropped and/or damaged and/or shows obvious signs of breakage.
- Disconnect the power supply cord before loosening the thumbscrews and always fasten the thumbscrews with a screwdriver before starting the system up.
- It is recommended that the device be installed only in a server room or computer room where access is:
  - Restricted to qualified service personnel or users familiar with restrictions applied to the location, reasons therefor, and any precautions required.
  - Only afforded by the use of a tool or lock and key, or other means of security, and controlled by the authority responsible for the location.

BURN HAZARD

Touching this surface could result in bodily injury. To reduce risk, allow the surface to cool before touching.

RISQUE DE BRÛLURES

Ne touchez pas cette surface, cela pourrait entraîner des blessures.
Pour éviter tout danger, laissez la surface refroidir avant de la toucher.

Getting Service

Ask an Expert: https://www.adlinktech.com/en/Askanexpert

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