cPCI-6940 Series

Server-grade 6U CompactPCI®
Intel® Xeon® D-1500 Processor Blade

User's Manual

Manual Rev.: 1.1

Revision Date: March 30, 2020

Part No: 50-15106-2010

Leading **EDGE COMPUTING**

Revision History

Revision	Release Date	Description of Change(s)
1.0	2018-02-01	Initial release
1.1	2020-03-30	Update memory installation instructions

Preface

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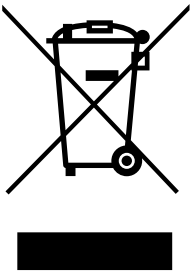

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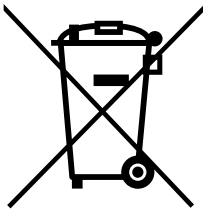

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Conventions

Take note of the following conventions used throughout this manual to make sure that users perform certain tasks and instructions properly.

NOTE: Additional information, aids, and tips that help users perform tasks.

CAUTION: Information to prevent ***minor*** physical injury, component damage, data loss, and/or program corruption when trying to complete a task.

WARNING: Information to prevent ***serious*** physical injury, component damage, data loss, and/or program corruption when trying to complete a specific task.

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1 Introduction

1.1 Overview

The ADLINK cPCI-6940 Series is a 6U CompactPCI® processor blade with Intel® Xeon® Processor D-1500 series. Intel® Xeon® Processor D-1500 family is based on 14nm silicon technology and integrates the CPU and chipset in a single system-on–chip (SoC). Powered by Intel® Xeon® Processor D-1500 SoC, the cPCI-6940 supports soldered DDR4-2133 ECC memory up to 16GB and socket type DDR4-2133 ECC memory up to 32GB. Total memory capacity is up to 48GB of DDR4-2133. In addition, the cPCI-6940 integrates an AMD Radeon™ E8860 embedded GPU to support outstanding graphics performance and up to 4 independent displays with one VGA and one DisplayPort on the faceplate and two digital signals to the rear. The cPCI-6940 is a powerful processor blade fit for mission critical applications in the military and aerospace industries.

The cPCI-6940 Series supports flexible IO interfaces with the cPCI-6940 in single-slot (4HP) and cPCI-6940D in dual slot (8HP) width form factors. Faceplate I/O for the cPCI-6940 includes 1x RJ-45 serial port, 1x DisplayPort, 1x VGA, 2x GbE supported by an Intel® 82580EB controller and 2x USB 3.0 ports. The cPCI-6940D is available in two SKUs, the cPCI-6940DH and cPCI-6940DX. In addition to the main board I/O, the cPCI-6940DH supports 2x 10G SFP+ ports and audio, while the cPCI-6940DX supports 2x 10G SFP+ ports, audio and 1x XMC space through PCIe x8 for I/O mezzanine card expansion. In terms of storage, the single-slot (4HP) cPCI-6940 provides space for 1x 2.5” SATA drive onboard and the dual-slot (8HP) cPCI-6940DH offers space for 1x additional 2.5” SATA drive on the daughter board. The 4HP and 8HP cPCI-6940 provide four additional SATA signals to rear J3 and J5.

Graphics support is provided by the AMD Radeon™ E8860 embedded GPU through PCIe x8 from the Intel® Xeon® Processor D-1500 SoC. It supports up to 4 independent displays with 1x DisplayPort, 1x VGA signal switchable to J3 and 2x DVI digital signals to J5.

Rear I/O signals to RTM include 2x GbE to J3 by Intel® 82580 GbE controllers for PICMG 2.16, 2x DVI to J5, 4x SATA 3 Gb/s* to J3 and J5, 2x USB 3.0 to J5, 4x USB 2.0 to J3, 5x GPIO, KB/MS, and 3x serial ports to J3 and J5. For PCIe expansion, the cPCI-6940 offers one PCIe x16 to J4 and one PCIe x4 to J5.

The ADLINK cPCI-6940 Series operates independently in both host and peripheral slots without CompactPCI bus communication (satellite mode), making it ideal for high density computing platforms. Moreover, the cPCI-6940 supports remote manageability by IPMI for system health monitoring over the Internet.

The cPCI-6940 Series offers powerful computing power based on the low power, high density Intel® Xeon® Processor D-1500 family, and is an ideal solution for military, aerospace and other robust computing applications that require highest computing power in a rugged, reliable CompactPCI system.

NOTE:

*Rear SATA can be upgraded to 6Gb/s by adding a redriver. Contact ADLINK if 6Gb/s is needed.

CAUTION:

The J4 pin-out is assigned for PCIe x16. The J4 PCIe x16 pin assignment is not compatible with PICMG 2.5 R1.0 Computer Telephony Specification. Therefore, do not insert the cPCI-6940 into the peripheral slot of a PICMG 2.5 H.110 compliant backplane in order to avoid causing serious damage to the cPCI-6940.

1.2 Features

- 6U CompactPCI blade in 4/8HP width form factor
- 14nm uFC-BGA Intel® Xeon® Processor D-1500 family
  - Intel® Xeon® processor D-1577, 16-core, 24M Cache, 1.30/2.1 GHz, 45W TDP
  - Intel® Xeon® processor D-1559, 12-core, 18M Cache, 1.50/2.1 GHz, 45W TDP, -40°C to 85°C
  - Intel® Xeon® processor D-1539, 8-core, 12M Cache, 1.60/2.2 GHz, 35W TDP, -40°C to 85°C
- One channel DDR4-2133 soldered SDRAM with ECC up to 16GB; one channel with two sockets SO-DIMM DDR4-2133 ECC memory up to 16+16GB
- Independent AMD Radeon™ E8860 embedded GPU, 128-bit wide, 2048MB, configuration type GDDR5, 72Gbps
- Supports up to 4 independent display
- One DisplayPort and one VGA port on faceplate, additional two DVI routed to rear
- 64-bit/66MHz CompactPCI Interface based on PCI specifications, universal V(I/O)
- Supports satellite mode operation in host and peripheral slots
- One PCIe x8 Gen2 XMC site on cPCI-6940DX
- Supports IPMI over LAN for system health monitoring
- Two Gigabit Ethernet egress ports on the faceplate provided by an Intel® 82580EB GbE controller via PCIe x1 and two additional Gigabit Ethernet ports routed to J3 (PICMG 2.16 compliant)
- Additional two Gigabit Ethernet ports with selected rear transition module (cPCI-R6100 Series)
- One 2.5” SATA drive space on the 4HP cPCI-6940 and one additional 2.5” SATA drive space on the 8HP cPCI-6940DH
- Four additional SATA signals to rear J3 and J5
- Atmel AT97SC3204 TPM support

1.3 Package Contents

The cPCI-6940 is packaged with the following components. If any of the following items are missing or damaged, retain the shipping carton and packing material and contact the dealer for inspection. Please obtain authorization before returning any product to ADLINK. The packing contents of cPCI-6940 Series non-standard configurations will vary depending on customer requests.

CPU module

- The cPCI-6940 Series Processor Blade
  - CPU and memory specifications will differ depending on options selected
  - Thermal module is assembled on the board
- DP-to-DVI adapter cable
- RJ-45 to DB-9 COM adapter cable
- 2.5" SATA drive accessory pack
- Additional SATA drive accessory pack for cPCI-6940DH

Rear Transition Module

- Dependent on the module selected

Optional Accessories

- DB-CFAST adapter board for CFast card assembly (contact ADLINK for ordering information)


NOTE:

The contents of non-standard cPCI-6940 configurations may vary depending on the customer's requirements.


CAUTION:

This product must be protected from static discharge and physical shock. Never remove any of the components except at a static-free workstation. Use the anti-static bag shipped with the product when putting the board on a surface. Wear an anti-static wrist strap properly grounded on one of the system's ESD ground jacks when installing or servicing system components.

2 Specifications

2.1 Processor Blade Specifications

CompactPCI® Standards	• PICMG® 2.0 CompactPCI® Rev. 3.0 • PICMG® 2.1 Hot Swap Specification Rev. 2.0 • PICMG® 2.9 System Management Rev. 1.0 • PICMG® 2.16 Packet Switching Backplane Rev. 1.0
Mechanical	• Standard 6U CompactPCI® • Board size: 233mm x 160mm • Single slot (4HP, 20.32mm) for cPCI-6940 • Dual-slot (8HP, 40.64mm) for cPCI-6940D • CompactPCI® HM (hard metric) connectors with J1, J2, J3 connector • J4 and J5 with UHM (ultra hard metric) connectors for high speed signals, optional HM (hard metric) connectors
Processor	• Intel® Xeon® processor D-1577, 16-core, 24M Cache, 1.30 GHz (2.1 GHz Turbo), 45W TDP • Intel® Xeon® processor D-1559, 12-core, 18M Cache, 1.50 GHz (2.1 GHz Turbo), 45W TDP, -40°C to 85°C • Intel® Xeon® processor D-1539, 8-core, 12M Cache, 1.60 GHz (2.2 GHz Turbo), 35W TDP, -40°C to 85°C • Passive heatsink
Chipset	• Integrated in CPU
Memory	• Dual channel 1.2V DDR4 2133MT/s SDRAM with ECC, 8Gb density support • Channel A: 2x 204-pin SO-DIMM socket, up to 16GB (32GB total) • Channel B: Soldered onboard, up to 16GB
CompactPCI Bus	• PCI 64-bit/66MHz; 3.3V, 5V universal V I/O • Supports operation in system slot as master • Supports operation in peripheral slot as standalone CPU board with non PICMG 2.5 H.110 compliant backplane
Gigabit Ethernet	• Two 10G SFP+ ports integrated on SoC (8HP versions only) • One PCIe x1 Intel® 82580EB GbE controller • Two egress 10/100/1000BASE-T ports on faceplate • Two egress 10/100/1000BASE-T ports routed to J3 for PICMG 2.16

Table 2-1: cPCI-6940 Processor Blade Specifications

Graphics	• Independent PCIe x8 AMD Radeon™ E8860 FCBGA embedded GPU, 128-bit wide, 2048MB, configuration type GDDR5, 72Gbps, 625 MHz graphics clock, DirectX 11.1, Open GL 4.2, Open CL 1.2 • Supports up to 4 independent displays • 37W thermal design power • One DisplayPort and one VGA port on faceplate, VGA switchable to J3 • Two additional DVI routed to rear J5
Serial Ports	• Up to four serial ports • One RS-232/422/485 serial port via RJ-45 connector on faceplate • One RS-232/422/485 serial port to J3 • One TX/RX to J3 and one TX/RX to J5
USB 2.0/3.0	• Two USB 3.0 ports on faceplate • Two USB 3.0 ports to J5 • Four USB 2.0 ports routed to J3
XMC	• One PCIe x8 Gen2 XMC site on cPCI-6940DX
PCIe	• 1x PCIe x4 Gen2 to J5, configurable to 4x PCIe x1 • 1x PCIe x16 to J4 Gen3*, configurable to 1x PCIe x8 to J4 and PCIe x8 to XMC on layer 2 by BIOS setting (p. 91) (*See note in “Block Diagrams” on page 8 below)
Audio	• High definition audio routed to faceplate for cPCI-6940D
TPM	Atmel AT97SC3204 TPM supporting: • Over/Under voltage detection • Low/High frequency sensor/filter • Reset filter • Memory encryption/decryption
Storage Interfaces[1]	• One onboard 2.5” SATA connector supporting SATA 6Gb/s drive on cPCI-6940 • Optional onboard 2.5" SATA 6Gb/s drive by adapter board for cPCI-6940DH • Four SATA 3Gb/s channels routed to J3 and J5
BIOS	• AMI® EFI BIOS, 64Mbit SPI flash memory, supports Configurable TDP • BIOS protection by jumper setting
OS Compatibility	• Windows Server 2012/2012 R2 • Windows 7 (64-bit), Windows 8.1 (64-bit) • Red Hat Enterprise Linux 6.4 (64-bit) • VxWorks 7 (32/64-bit) • Other OS support upon request

Table 2-1: cPCI-6940 Processor Blade Specifications

Faceplate I/O	**cPCI-6940 (4HP)** • 1x RJ-45 serial port • 1x DisplayPort • 1x VGA port • 2x 10/100/1000BASE-T Ethernet ports • 2x USB 3.0 ports **cPCI-6940DH (8HP)** • 1x RJ-45 serial port • 1x DisplayPort • 1x VGA port • 2x 10/100/1000BASE-T Ethernet ports • 2x USB 3.0 ports • 2x 10G SFP+ ports • 1x Mic-in and 1x Line-out **cPCI-6940DX (8HP)** • 1x RJ-45 serial port • 1x DisplayPort • 1x VGA port • 2x 10/100/1000BASE-T Ethernet ports • 2x USB 3.0 ports • 2x 10G SFP+ ports • 1x Mic-in and 1x Line-out • 1x XMC site
Environmental	• Operating Temperature (with forced air flow)[1]: Standard: -20°C to +60°C (D-1577 SKU) -20°C to +70°C (D-1559, D-1539 SKUs) Extreme: -40°C to +85°C (D-1559, D-1539 SKUs, screened) • Storage Temperature: -50°C to 100°C • Humidity: 95% @60°C non-condensing • Shock: 20G peak-to-peak, 11ms duration, non-operating • Vibration[2]: 3.5Grms, 5-500Hz, each axis, operating (w/o hard drive)
EMI	• CE EN55022 • FCC Class A

Table 2-1: cPCI-6940 Processor Blade Specifications

1. ADLINK-certified thermal design. The thermal performance is dependent on the chassis cooling design. Sufficient forced air-flow is required. Temperature limits of optional mass storage devices may also affect the thermal specification.
2. The storage device limits the operational vibration tolerance. When the application requires higher specification for anti-vibration, it is recommended to use a flash storage device.

2.2 Block Diagrams

cPCI-6940 Processor Blade

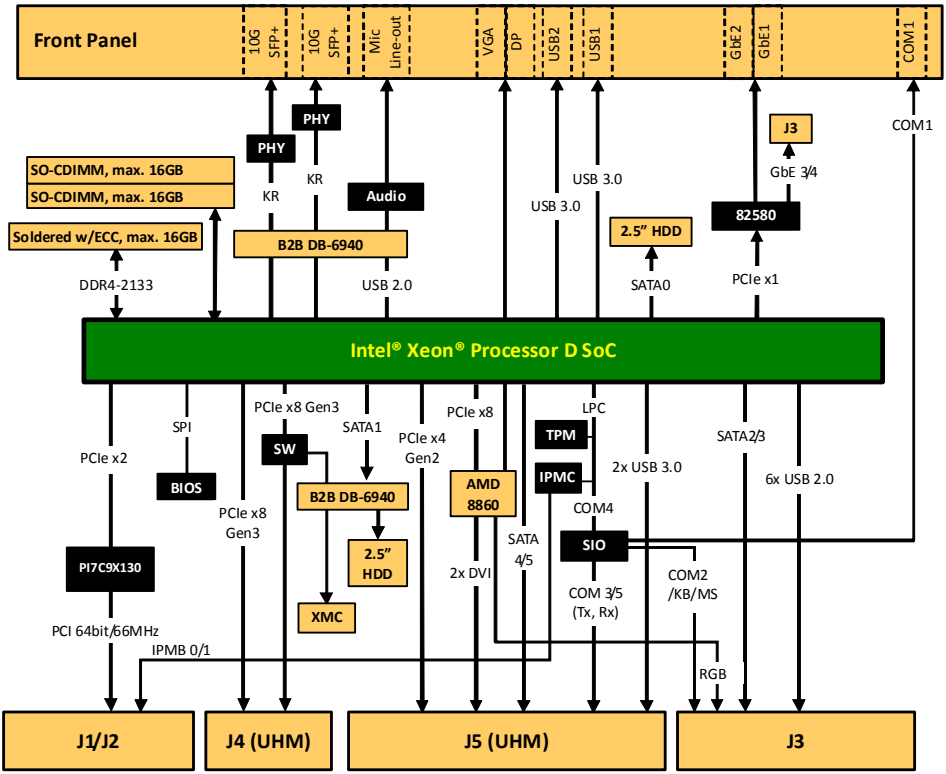

Figure 2-1: cPCI-6940 Processor Blade Functional Block Diagram

NOTE:

PCIe x16 from the SoC is Gen3, but due to signal routing and connector limitations, a redriver is required to ensure PCIe Gen3 speed at the rear I/O.

PCIe x16 supports Gen1 only when mated with cPCI-R66X0 Series due to lack of redriver on these RTMs.

2.3 I/O Connectivity Table

Function	cPCI-6940 (4HP)		cPCI-6940DX (8HP)		cPCI-6940DH (8HP)	
	Faceplate	Onboard	Faceplate	Onboard	Faceplate	Onboard
Gigabit Ethernet	Y x2		Y x2		Y x2	
COM	Y (RJ-45)		Y (RJ-45)		Y (RJ-45)	
USB3.0	Y x2		Y x2		Y x2	
USB 2.0						
DisplayPort	Y x1		Y x1		Y 1x	
VGA	Y x1		Y x1		Y x1	
Serial ATA		Y x1		Y x1		Y x2
CFast						
XMC				Y x1		
10G SFP+			Y x2		Y x2	
Audio (Mic-in, Line-out)			Y x1		Y x1	
LEDs	Y x5		Y x5		Y x5	

Table 2-2: cPCI-6940 I/O Connectivity

2.4 Power Requirements

In order to guarantee a stable functionality of the system, it is recommended to provide more power than the system requires. **An industrial power supply unit should be able to provide at least twice as much power as the entire system requires of each voltage**. An ATX power supply unit should be able to provide at least three times as much power as the entire system requires of each voltage.

The tolerance of the voltage lines described in the CompactPCI specification (PICMG 2.0 R3.0) is +5%/-3% for 5, 3.3 V and ±5% for ±12V. This specification is for power delivered to each slot and it includes both the power supply and the backplane tolerance.

Voltage	Nominal Value	Tolerance	Max. Ripple (P - P)
5V	+5.0 VDC	+5% / -3%	50 mV
3.3V	+3.3 VDC	+5% / -3%	50 mV
+12V	+12 VDC	+5% / -5%	240 mV
-12V	-12 VDC	+5% / -5%	240 mV
V I/O (PCI I/O Buffer Voltage)	+3.3 VDC or +5 VDC	+5% / -3%	50 mV
GND			

Power Consumption

This section provides information on the power consumption of cPCI-6940 Series when using Intel® Xeon® Processor D-1500 family with 16GB DDR4-2133 ECC soldered memory and two 4GB DDR4-2133 ECC socket memory module. Storage device is used with ADLINK ASD26-MLC64G-CT 64GB SATA SSD. The cPCI-6940 is powered by 5V and 3.3V. Power consumption at 100% CPU usage was measured by running Intel Thermal Analysis Tool (TAT) and Power Thermal Utility (PTU) Rev. 1.2, under Windows 7 Ultimate SP1 x64, with BIOS EIST Enabled and cTDP Normal.

Intel® Xeon® Processor D-1577 (24M cache, 1.30 GHz, 45W)			
OS/Mode	**Current 3.3V**	**Current 5V**	**Total Power**
Windows 7, Idle mode	2.37 A	2.65 A	20.84 W
Windows 7, Typical mode	5.24 A	12.7 A	80.80 W
Windows 7, Max mode	5.09 A	11.3 A	73.28 W

Intel® Xeon® Processor D-1559 (18M cache, 1.50 GHz, 45W)			
OS/Mode	**Current 3.3V**	**Current 5V**	**Total Power**
Windows 7, Idle mode	2.30 A	2.84 A	21.79 W
Windows 7, Typical mode	5.13 A	12.25 A	78.18 W
Windows 7, Max mode	4.78 A	11.08 A	71.17 W

Intel® Xeon® Processor D-1539 (12M cache, 1.60 GHz, 35W)			
OS/Mode	**Current 3.3V**	**Current 5V**	**Total Power**
Windows 7, Idle mode	2.30 A	2.40 A	19.59 W
Windows 7, Typical mode	5.27 A	9.99 A	67.34 W
Windows 7, Max mode	4.95 A	8.33 A	57.99 W

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3 Functional Description

The following sections describe the cPCI-6940 Series features and functions.

3.1 Processors

The Intel® Xeon® Processor D-1500 family the first Intel® Xeon® SoC based on 14nm silicon technology. The Intel® Xeon® processor D-1500 product family is the first offering of a line of processors that will address a broad rand of low-power, high-density application needs. The SoC has an integrated platform controller hub (PCH), integrated I/O, two integrated 10 Gigabit Intel® Ethernet ports, and a wide ranging thermal design power (TDP). The Intel® Xeon® Processor D-1500 family provides excellent performance and software compatibility in a low-power SoC that is ideal as a micro-server in mission critical CompactPCI® platforms.

Features	D-1577	D-1559	D-1539
Clock	1.3 GHz	1.5 GHz	1.6 GHz
Max. Single Core Turbo Freq.	2.1 GHz	2.1 GHz	2.2 GHz
Last Level Cache	24MB	18MB	12MB
No. of Core(s)	16/32	12/24	8/16
Max. Power (TDP[1])	45 W	45 W	35 W
$T_{Case-MAX}$[2]	94°C	91°C	92°C
Operating Temperature Range (ambient)	0°C to 60°C	-40°C to 85°C	-40°C to 85°C

1. The highest expected sustainable power while running known power intensive applications. TDP is not the maximum power that the processor can dissipate.
2. The maximum supported case temperature.

Supported Technologies

Features	D-1577	D-1559	D-1539
Intel® Virtualization Technology for Directed I/O (Intel® VT-d)	Yes	Yes	Yes
Intel® Virtualization Technology (Intel® VT-x)	Yes	Yes	Yes
Intel® VT-x with Extended Page Tables (EPT)	Yes	Yes	Yes
Intel® Hyper-Threading Technology	Yes	Yes	Yes
Intel® 64 Architecture	Yes	Yes	Yes
Execute Disable Bit	Yes	Yes	—
Intel® Turbo Boost Technology	2.0	2.0	2.0
Intel® TSX-NI	Yes	Yes	Yes
Enhanced Intel® SpeedStep® Technology	Yes	Yes	Yes
Thermal Monitoring Technologies	Yes	Yes	Yes

Interfaces

- Intel® Xeon® Processor D-1500 family built in integrated memory controller
- Two channels of DDR4-2133 ECC memory, up to 2 DIMMs per channel
- DDR4 data transfer rates of 1600/1867/2133 MT/s
- 64-bit wide channels
- DDR4 I/O Voltage of 1.2V
- 8Gb x8 DDR4 DRAM technologies supported, the largest memory capacity possible is 16 GB
- PCI Express ports are fully-compliant with the PCI Express Base Specification, Revision 2.0 and Revision 3.0.

3.2 Chipset

The Intel® Xeon® Processor D-1500 family integrates a platform controller hub (PCH) in the SoC

3.3 Graphics

The cPCI-6940 is equipped with the AMD Radeon™ E8860 embedded graphics processor that is the first embedded GPU developed on the groundbreaking Graphics Core Next (GCN) architecture. The AMD Radeon E8860 GPU delivers industry-leading 3D video graphics performance, enabling stunning, multi-display visual experiences for a range of embedded applications. The AMD Radeon E8860 GPU is based on 28nm silicon technology with 625 MHz graphics clock and features 2GB, 1125 MHz Frame Buffer GDDR5. The AMD Radeon E8860 GPU supports DirectX 11.1, OpenGL 4.2, and OpenC 1.2, enabling high-performance graphics and massive parallel processing. The AMD Radeon E8860 GPU has a thermal design power of 37W and has an integrated thermal sensor for GPU protection.

3.4 XMC

The cPCI-6940DX model provides one XMC site for faceplate I/O expansion. The XMC site provides PCI-Express x8 Gen2 lanes which are supported by a PCIe x8 switch. See “IIO PCIe Port 3” on page 91 in the BIOS chapter for information on how to set the switch.

3.5 Intel® Turbo Boost Technology

Intel® Turbo Boost Technology is a feature that allows the processor to opportunistically and automatically run faster than its rated operating core and/or render clock frequency when there is sufficient power headroom, and the product is within specified temperature and current limits. The Intel Turbo Boost Technology feature is designed to increase performance of both multi-threaded and single-threaded workloads. The processor supports a Turbo mode where the processor can use the thermal capacity associated with package and **run at power levels higher than TDP power for short durations**. This improves the system responsiveness for short, bursty usage conditions.

Turbo Mode availability is independent of the number of active cores; however, the Turbo Mode frequency is dynamic and dependent on the instantaneous application power load, the number of active cores, user configurable settings, operating environment, and system design. If the power, current, or thermal limit is reached, the processor will automatically reduce the frequency to stay with its TDP limit.

3.6 Intel® Hyper-Threading Technology

Intel® Hyper-Threading Technology allows an execution core to function as two logical processors. While some execution resources (such as caches, execution units, and buses) are shared, each logical processor has its own architectural state with its own set of general-purpose registers and control registers. This feature must be enabled using the BIOS and requires operating system support. Intel recommends enabling Hyper-Threading Technology with Microsoft Windows 7, Vista, and XP, and disabling Hyper-Threading Technology using the BIOS for all previous versions of Windows operating systems.

3.7 Trusted Platform Module

The cPCI-6940 integrates an Atmel AT97SC3204 Trusted Platform Module (TPM). The TPM is a secure controller with added cryptographic functionality to provide users a secure environment in e-commerce transactions and Internet communications.

The key features Trusted Platform Module (TPM) offers are:

- Fully compliant to the Trusted Computing Group (TCG) Trusted Platform Module (TPM) version 1.2 specification
- Hardware hash accelerator for SHA-1 algorithm
- Advanced Crypto Engine (ACE) for asymmetric key operations(up to 2048-bit key length) to make hardware protection.
- Tick counter to extend the time required to decipher the key
- In addition to encryption key created by user. it also provide some security features to protect the integrated circuit itself:
- Over/Under-voltage detection to monitor the system stability. If the voltage fluctuates dramatically, this function can block the data transfer and lock the chip.

- Low/High frequency sensor to detect the IC clock frequency. If the frequency fluctuates dramatically, this function can block the data transfer and lock the chip.
- Reset filter to filter reset signal in order to break the time set by tick counter is received
- Memory encryption to protect memory
- Physical shield in the IC to protect the die from intruding or hacking by matching the data transferred on the 2 layer metal shield on the IC. If the data is not matched, the IC may be blocked.

3.8 Battery

The cPCI-6940 is equipped with a 3.0V "coin cell" lithium battery for the Real Time Clock (RTC). The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer. A BR2032 battery is equipped on board by default.

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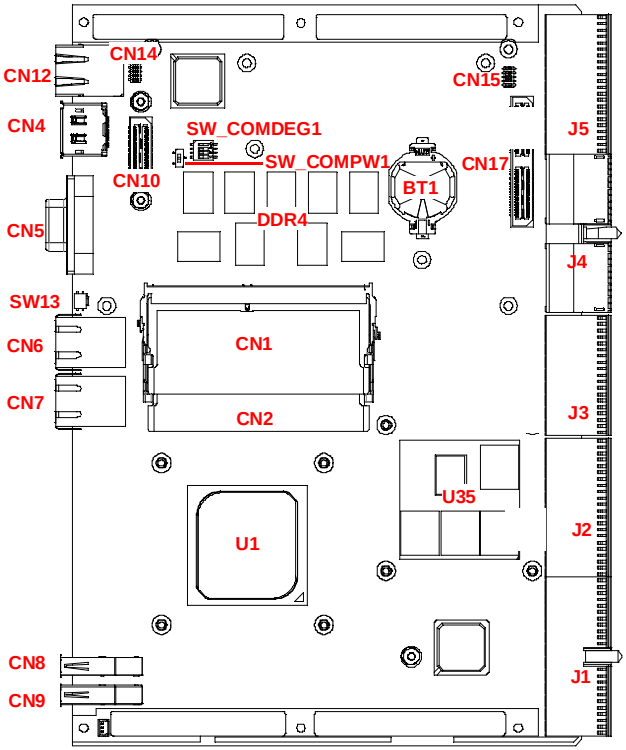
4 Board Interfaces

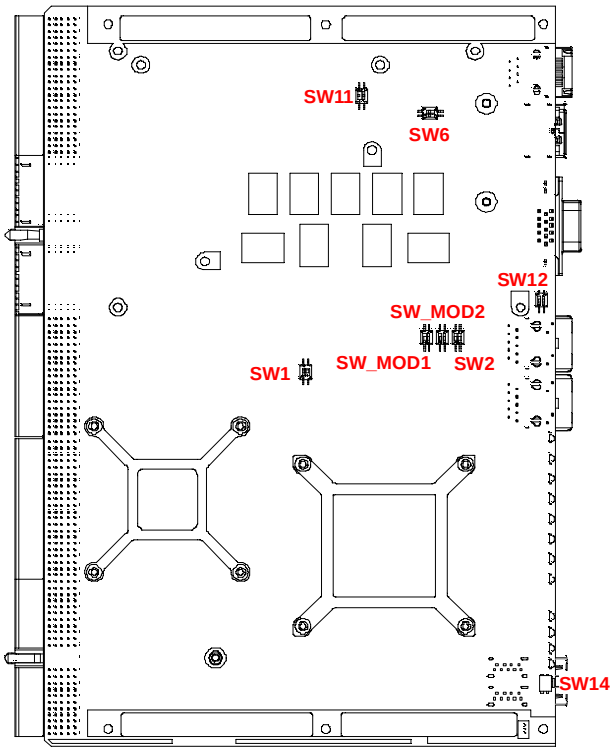
This chapter illustrates the board layout, connector pin assignments, and jumper settings to familiarize users with the cPCI-6940 Series.

4.1 cPCI-6940 Series Board Layout



U1	Xeon processor D	**J1-J5**	CompactPCI connectors
U35	Radeon E8860 GPU	**CN5**	VGA connector
CN1/2	DDR4 SO-DIMMs	**CN12**	RJ-45 serial port
CN8/9	USB 3.0 connectors	**CN17**	Board-to-board connector
CN4	DisplayPort connector	**SW13**	RTC reset button
CN6/7	GbE ports	**SW_COMPW1**	Reserved
CN10	SATA adapter connector	**SW_COMDEG1**	Reserved
CN14/15	Reserved	**BT1**	Battery socket

Figure 4-1: cPCI-6940 Series Board Layout - Component Side



SW1	BIOS protection	**SW2**	VGA front/rear switch
SW6	Serial port CN12 mode control	**SW11**	Reserved
SW12	Reserved	**SW14**	System reset button
SW_MOD1	Reserved	**SW_MOD2**	Reserved

Figure 4-2: cPCI-6940 Series Board Layout - Solder Side

4.2 cPCI-6940 Series Assembly Layout

cPCI-6940

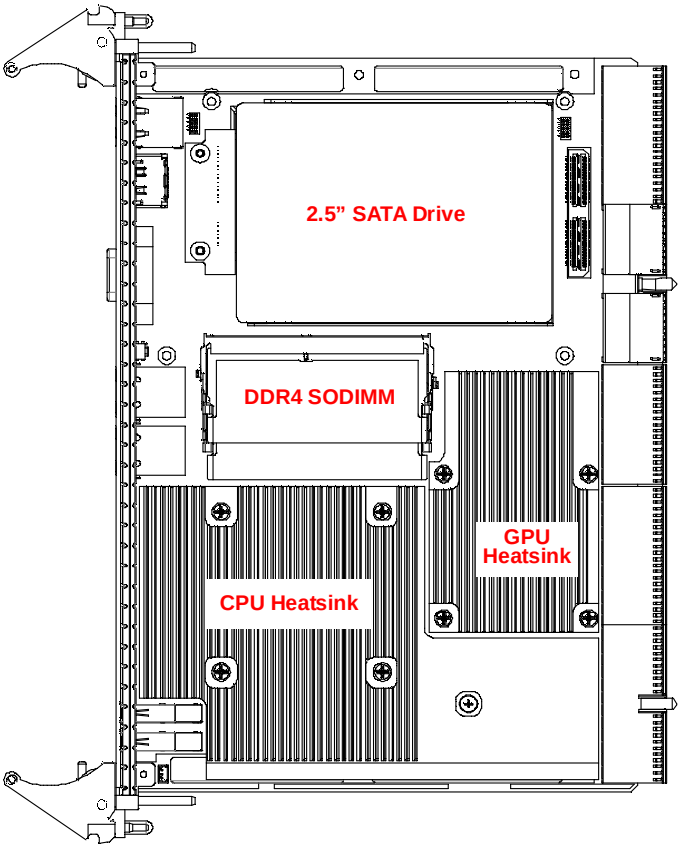


Figure 4-3: cPCI-6940 Assembly Layout

cPCI-6940DH

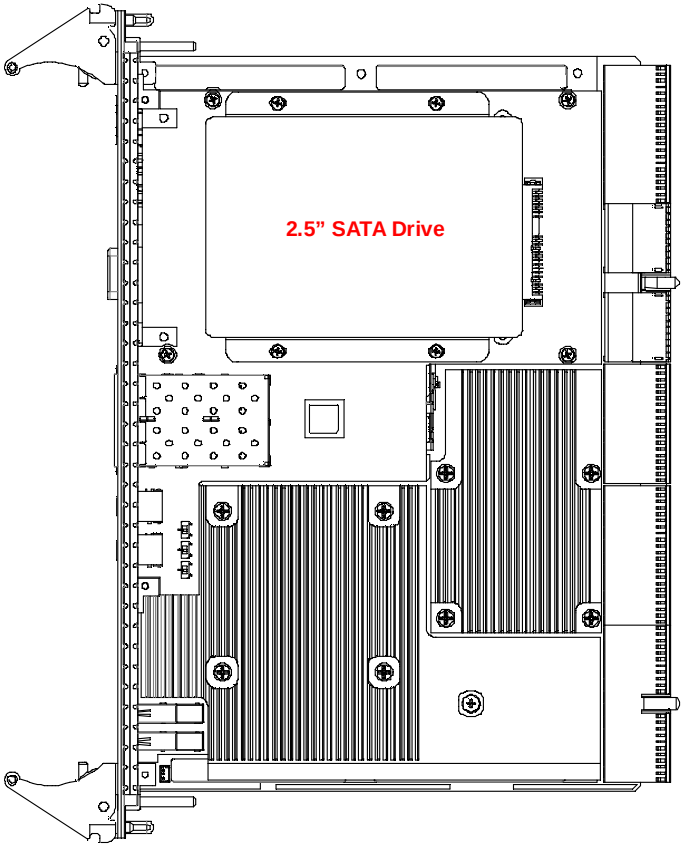


Figure 4-4: cPCI-6940DH Assembly Layout

cPCI-6940DX

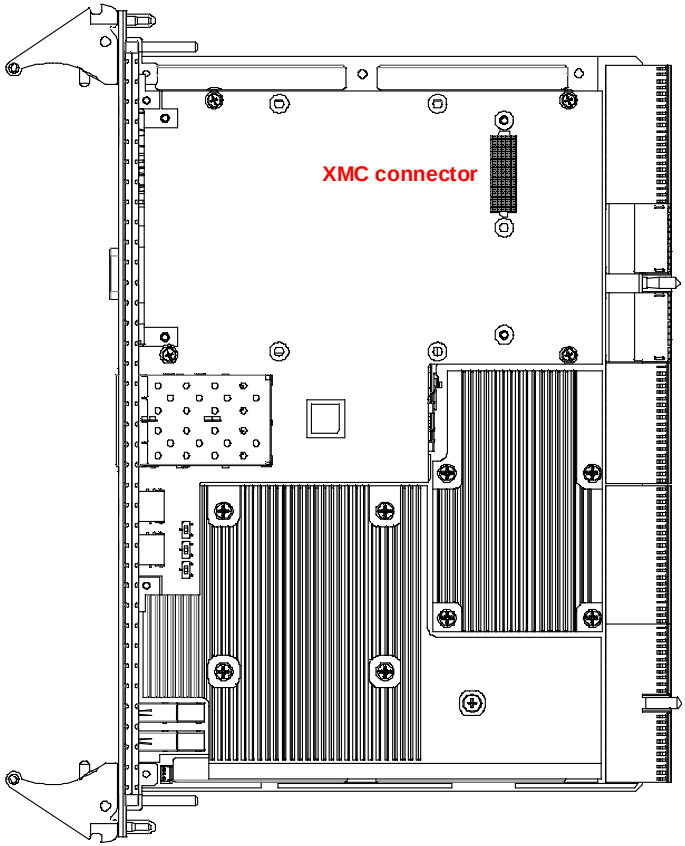
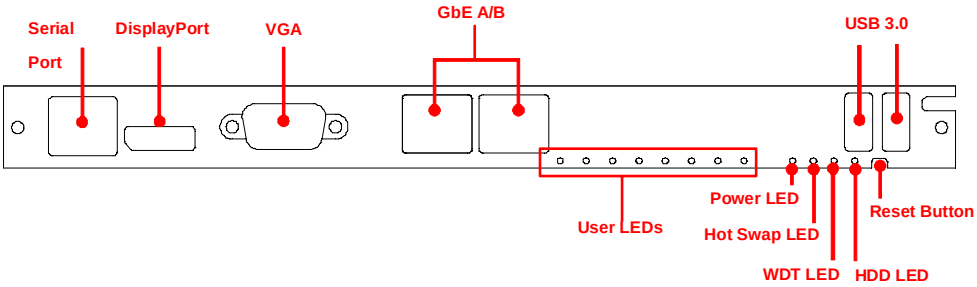


Figure 4-5: cPCI-6940DX Assembly Layout

4.3 cPCI-6940 Series Faceplate

cPCI-6940 Faceplate



cPCI-6940DH/DX Faceplate

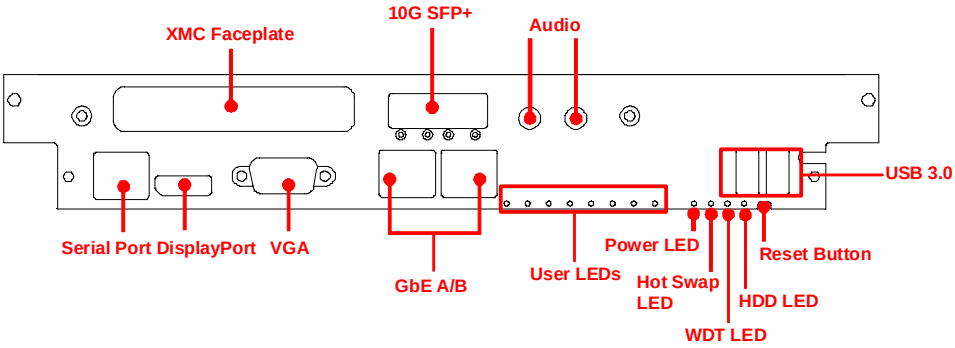


Figure 4-6: cPCI-6940 Series Faceplate Layout

NOTE:

The cPCI-6940DH/DX uses the same faceplate design. For cPCI-6940DH with 2.5" SATA drive onboard, the XMC space cannot be used simultaneously

System LEDs

LED	Color	Condition	Indication
Power 	Green	OFF	System is off
		Red	System Power ready (PWGD)
		Green	Post OK
WDT* 	Red	OFF	No Watchdog event
		Blinking	Watchdog event alert
HDD 	Yellow	OFF	No SATA drive activity
		Blinking	Data read/write in process for SATA drive
Hot Swap 	Blue	Off	Handles closed, system is on
		Fast Blink	Preparing to shut down system (LED: 0.1s on, 0.9s off.)
		On	Handles open and blade ready to be removed
		Slow Blink	Voltages out of tolerance: 3.3V, 5V, 12V, 1.5V over ±5% (LED: 2s on, 1s off)

Table 4-1: cPCI-6940 Faceplate System LED Descriptions

*The WDT LED is connected to the GPIO pins of the IPMC. The WDT LED can be programmed by the user as a general purpose LED. Please contact ADLINK for sample code.

User LEDs

The eight User LEDs on the front panel display port 80h POST codes in hexadecimal during boot up. Users can use the POST codes to identify issues during the BIOS POST process. In default mode, these eight LEDs display the POST code output to Port 80h during system bootup. For example, if the Bit7 > Bit0 output is “01110101”, then the port 80h output is “75h” (see “Checkpoints & Beep Codes” on page 107).

Each LED indicates a corresponding bit of the port 80h POST code. Refer to the figure and table below.

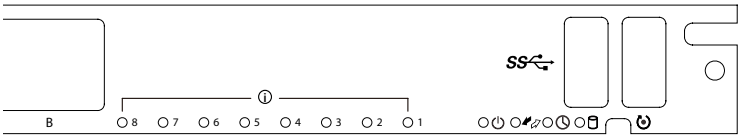


Figure 4-7: cPCI-6940 Series LED Labels

LED 1	Port 80h bit0
LED 2	Port 80h bit1
LED 3	Port 80h bit2
LED 4	Port 80h bit3
LED 5	Port 80h bit4
LED 6	Port 80h bit5
LED 7	Port 80h bit6
LED 8	Port 80h bit7

For assistance using the User LEDs, please log in to: **http://askanexpert.adlinktech.com**.

4.4 Connector Pin Assignments

COM (RJ-45)

Pin #	RS-232	RS-422	RS-485
1	DCD#	TX-	Data-
2	RTS#	—	—
3	DSR#	—	—
4	TXD	RX+	—
5	RXD	TX+	Data+
6	GND	—	—
7	CTS#	—	—
8	DTR#L	RX-	—

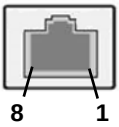


Table 4-2: Faceplate COM Pin Definitions

COM RJ-45 to DB-9 Cable

Pin #	RS-232	RS-422	RS-485
1	DCD#	TX-	Data-
2	RXD	TX+	Data+
3	TXD	RX+	—
4	DTR#L	RX-	—
5	GND	—	—
6	DSR#	—	—
7	RTS#	—	—
8	CTS#	—	—
9	—	—	—

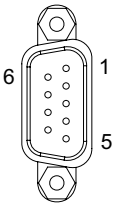


Table 4-3: COM RJ-45 to DB-9 Cable Pin Definitions

DisplayPort Connector

Pin #	Signal	Pin #	Signal
1	CN_DP0_P	2	Ground
3	CN_DP0_N	4	CN_DP1_P
5	Ground	6	CN_DP1_N
7	CN_DP2_P	8	Ground
9	CN_DP2_N	10	CN_DP3_P
11	Ground	12	CN_DP3_N
13	CN_CAD-L	14	CN_CEC
15	CN_AUX_P	16	Ground
17	CN_AUX_N	18	DDP_HPD
19	Ground	20	P3V3

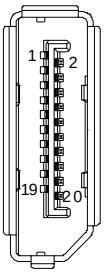


Table 4-4: DisplayPort Connector Pin Definition

VGA Connector

Signal Name	Pin #	Pin #	Signal Name
Red	1	2	Green
Blue	3	4	N.C.
GND	5	6	GND
GND	7	8	GND
+5V.	9	10	GND
N.C.	11	12	CRTDATA
HSYNC	13	14	VSYNC
CRTCLK	15		

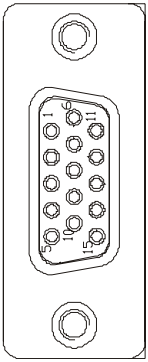


Table 4-5: VGA Connector Pin Definition

USB 3.0 Connectors

Pin #	Signal Name
1	USB3.0_P5VA
2	USB2_CMAN
3	USB2_CMAP
4	GND
5	USB3A_CMRXN
6	USB3A_CMRXP
7	GND
8	USB3A_CMTXN
9	USB3A_CMTXP

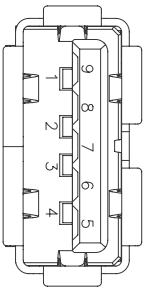
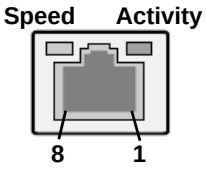


Table 4-6: USB 3.0 Connector Pin Definition

RJ-45 Gigabit Ethernet Connectors

Pin #	GbE A/B
1	TD0+
2	TD0-
3	TD1+
4	TD2+
5	TD2-
6	TD1-
7	TD3+
8	TD3-

Table 4-7: RJ-45 GbE Pin Definitions



Status		Speed LED (Green/Orange)	Activity LED (Yellow)
Network link is not established or system powered off		OFF	OFF
10 Mbps	Link	OFF	ON
	Active	OFF	Blinking
100 Mbps	Link	Green	ON
	Active	Green	Blinking
1000 Mbps	Link	Orange	ON
	Active	Orange	Blinking

Table 4-8: LAN LED Status Definitions

SFP+ 10Gigabit Ethernet Connector (8HP versions only)

Pin #	1000BASE-T
1	GND
2	SFP_TX_FAULT
3	SFP_TX_DISABLE
4	SFP_SDA
5	SFP_SCL
6	SFP_MOD_ABS
7	GND
8	SFP_RX_LOS
9	GND
10	GND
11	GND
12	SRDS_RX-N
13	SRDS_RX-P
14	GND
15	SFP_V3P3_R
16	SFP_V3P3_T
17	GND
18	SRDS_TX-P
19	SRDS_TX-N
20	GND

Serial ATA Connector with Power

Pin #	Signal
S1	GND
S2	TX+
S3	TX-
S4	GND
S5	RX-
S6	RX+
S7	GND
P1	NC
P2	NC
P3	NC
P4	GND
P5	GND
P6	GND
P7	5V
P8	5V
P9	5V
P10	GND
P11	NC
P12	GND
P13~P15	NC

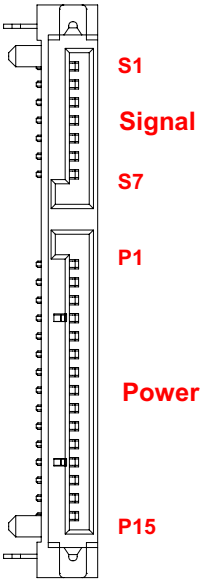


Table 4-9: Serial ATA Connector with power Pin Definition

CFast Socket (on optional DB-CFAST adapter board)

Pin #	Signal Name
Ground	S1
SATA_TX-P	S2
SATA_TX-N	S3
Ground	S4
SATA_RX-N	S5
SATA_RX-P	S6
Ground	S7
CFast_CDI	P1
Ground	P2
NC	P3
NC	P4
NC	P5
NC	P6
Ground	P7
CFast_LED1	P8
CFast_LED2	P9
NC	P10
NC	P11
NC	P12
+3.3V	P13
+3.3V	P14
Ground	P15
Ground	P16
CFast_CDO	P17

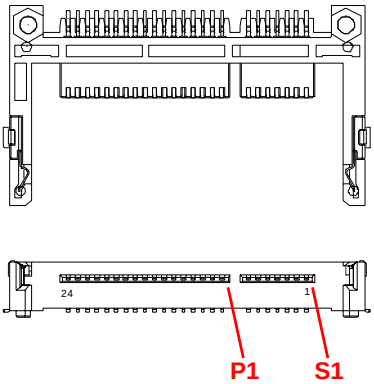
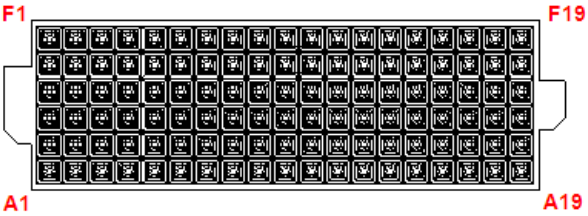


Table 4-10: CFast Socket Pin Definition

XMC Connector



Pin#	A	B	C	D	E	F
1	RXP	RXN	3.3V	NC	NC	VPWR
2	GND	GND	Not used	GND	GND	PCIE_RST-L
3	NC	NC	3.3V	NC	NC	VPWR
4	GND	GND	Not used	GND	GND	Not used
5	NC	NC	3.3V	NC	NC	VPWR
6	GND	GND	Not used	GND	GND	+12V
7	NC	NC	3.3V	NC	NC	VPWR
8	GND	GND	Not used	GND	GND	-12V
9	NC	NC	Not used	NC	NC	VPWR
10	GND	GND	Not used	GND	GND	GA0
11	TXP	TXN	Not used	NC	NC	VPWR
12	GND	GND	GA1	GND	GND	Not used
13	NC	NC	3.3V	NC	NC	VPWR
14	GND	GND	GA2	GND	GND	Not used
15	NC	NC	Not used	NC	NC	VPWR
16	GND	GND	Not used	GND	GND	Not used
17	NC	NC	Not used	NC	NC	NC
18	GND	GND	Not used	GND	GND	Not used
19	CK-P	CK-N	Not used	Not used	Not used	Not used

Table 4-11: XMC Connector Pin Definition

CompactPCI J1 Connector

Pin	Z	A	B	C	D	E	F
25	GND	P5V	CPCI_REQ64-L	CPCI_ENUM-L	P3V3	P5V	GND
24	GND	CPCI_AD1	P5V	V(I/O)	CPCI_AD0	CPCI_ACK64-L	GND
23	GND	P3V3	CPCI_AD4	CPCI_AD3	P5V	CPCI_AD2	GND
22	GND	CPCI_AD7	GND	P3V3	CPCI_AD6	CPCI_AD5	GND
21	GND	P3V3	CPCI_AD9	CPCI_AD8	CPCI_M66EN	CPCI_CBE-L0	GND
20	GND	CPCI_AD12	GND	VIO	CPCI_AD11	CPCI_AD10	GND
19	GND	P3V3	CPCI_AD15	CPCI_AD14	GND	CPCI_AD13	GND
18	GND	CPCI_SERR-L	GND	P3V3	CPCI_PAR	CPCI_CBE-L1	GND
17	GND	P3V3	IPMB_CLK	IPMB_DAT	GND	CPCI_PERR-L	GND
16	GND	CPCI_DEVSEL-L	GND	VIO	CPCI_STOP-L	CPCI_LOCK-L	GND
15	GND	P3V3	CPCI_FRAME-L	CPCI_IRDY-L	CPCI_BDSEL-L	CPCI_TRDY-L	GND
12-14	Key	Key Area					Key
11	GND	CPCI_AD18	CPCI_AD17	CPCI_AD16	GND	CPCI_CBE-L2	GND
10	GND	CPCI_AD21	GND	P3V3	CPCI_AD20	CPCI_AD19	GND
9	GND	CPCI_CBE-L3	CPCI_IDSEL	CPCI_AD23	GND	CPCI_AD22	GND
8	GND	CPCI_AD26	GND	VIO	CPCI_AD25	CPCI_AD24	GND
7	GND	CPCI_AD30	CPCI_AD29	CPCI_AD28	GND	CPCI_AD27	GND
6	GND	CPCI_REQ-L0	CPCI_PRESENT-L	P3V3	CPCI_CLK0	CPCI_AD31	GND
5	GND	NC	NC	CPCI_RESET-L	GND	CPCI_GNT-L0	GND
4	GND	P5V_IPMB	IPMC_HEALTHY-L	VIO	VIO	VIO	GND
3	GND	CPCI_INTA-L	CPCI_INTB-L	CPCI_INTC-L	P5V	CPCI_INTD-L	GND
2	GND	CPCI_TCK*	P5V	CPCI_TMS*	CPCI_TDO*	CPCI_TDI*	GND
1	GND	P5V	N12V	TRST#*	P12V	P5V	GND

Table 4-12: CompactPCI J1 Connector Pin Definition

*Not implemented

CompactPCI J2 Connector

Pin	Z	A	B	C	D	E	F
22	GND	GA4	GA3	GA2	GA1	GA0	GND
21	GND	CPCI_CLK6	GND	NC	NC	NC	GND
20	GND	CPCI_CLK5	GND	NC	GND	NC	GND
19	GND	GND	GND	IPMB_DAT	IPMB_CLK	P3V3_AUX	GND
18	GND	NC	NC	NC	GND	NC	GND
17	GND	NC	GND	J2_RSTBTN-L	CPCI_REQ-L6	CPCI_GNT-L6	GND
16	GND	NC	NC	CPCI_DEGL	GND	NC	GND
15	GND	NC	GND	CPCI_FAL-L	CPCI_REQ-L5	CPCI_GNT-L5	GND
14	GND	CPCI_AD35	CPCI_AD34	CPCI_AD33	GND	CPCI_AD32	GND
13	GND	CPCI_AD38	GND	VIO	CPCI_AD37	CPCI_AD36	GND
12	GND	CPCI_AD42	CPCI_AD41	CPCI_AD40	GND	CPCI_AD39	GND
11	GND	CPCI_AD45	GND	VIO	CPCI_AD44	CPCI_AD43	GND
10	GND	CPCI_AD49	CPCI_AD48	CPCI_AD47	GND	CPCI_AD46	GND
9	GND	CPCI_AD52	GND	VIO	CPCI_AD51	CPCI_AD50	GND
8	GND	CPCI_AD56	CPCI_AD55	CPCI_AD54	GND	CPCI_AD53	GND
7	GND	CPCI_AD59	GND	VIO	CPCI_AD58	CPCI_AD57	GND
6	GND	CPCI_AD63	CPCI_AD62	CPCI_AD61	GND	CPCI_AD60	GND
5	GND	CPCI_CBE-L5	CPCI_DEV64-L	VIO	CPCI_CBE-L4	CPCI_PAR64	GND
4	GND	VIO	NC	CPCI_CBE-L7	GND	CPCI_CBE-L6	GND
3	GND	CPCI_CLK4	GND	CPCI_GNT-L3	CPCI_REQ-L4	CPCI_GNT-L4	GND
2	GND	CPCI_CLK2	CPCI_CLK3	SYSEN-L	CPCI_GNT-L2	CPCI_REQ-L3	GND
1	GND	CPCI_CLK1	GND	CPCI_REQ-L1	CPCI_GNT-L1	CPCI_REQ-L2	GND

Table 4-13: CompactPCI J2 Connector Pin Definition

CompactPCI J3 Connector

Pin	Z	A	B	C	D	E	F
19	GND	P5V	P5V	P12V	P5V	P5V	GND
18	GND	LAN4_TXDP0	LAN4_TXDN0	GND	LAN4_TXDP2	LAN4_TXDN2	GND
17	GND	LAN4_TXDP1	LAN4_TXDN1	GND	LAN4_TXDP3	LAN4_TXDN3	GND
16	GND	LAN3_TXDP0	LAN3_TXDN0	GND	LAN3_TXDP2	LAN3_TXDN2	GND
15	GND	LAN3_TXDP1	LAN3_TXDN1	GND	LAN3_TXDP3	LAN3_TXDN3	GND
14	GND	USB_OC3#	USB_OC4#	USB_OC5#	USB_OCA#	USB_OCB#	GND
13	GND	U2_DAP	U2_DAN	GND	U2_DBP	U2_DBN	GND
12	GND	U2_D4P	U2_D4N	GND	U2_D5P	U2_D5N	GND
11	GND	U2_D2P	U2_D2N	GND	U2_D3P	U2_D3N	GND
10	GND	USB_OC2#	CRT_DDC_CLK	CRT_DDC_DATA	CRT_HSYNC	CRT_VSYNC	GND
9	GND	COM2_CTS-L	COM2_RI-L	CRT_BLUE	CRT_RED	CRT_GREEN	GND
8	GND	COM2_RX	COM2_TX	COM2_DTR-L	COM2_DSR-L	COM2_RTS-L	GND
7	GND	COM3_TX	COM3_RX	COM2-DCD-L	IPMB_CLK	IPMB_DAT	GND
6	GND	SATA-RXP4	SATA-RXN4	GND	SATA-RXP3	SATA-RXN3	GND
5	GND	GND	GND	NC	GND	GND	GND
4	GND	SATA-TXP4	SATA-TXN4	GND	SATA-TXP3	SATA-TXN3	GND
3	GND	KBDATA	KBCLK	NC	MSDATA	MSCLK	GND
2	GND	NC	NC	NC	NC	NC	GND
1	GND	NC	NC	NC	NC	NC	GND

Table 4-14: CompactPCI J3 Connector Pin Definition

CompactPCI J4 Connector

Pin	Z	A	B	C	D	E	F
25	GND	NC	PCIE_J4_TXP15	GND	PLTRST_PCIEX16	PCIE_WAKE-L	GND
24	GND	GND	PCIE_J4_TXN15	PCIE_J4_RXP13	NC	GND	GND
23	GND	PCIE_J4_TXP13	GND	PCIE_J4_RXN13	GND	PCIE_J4_RXP15	GND
22	GND	PCIE_J4_TXN13	PCIE_J4_TXP14	GND	PCIE_J4_RXP14	PCIE_J4_RXN15	GND
21	GND	GND	PCIE_J4_TXN14	PCIE_J4_TXP12	PCIE_J4_RXN14	GND	GND
20	GND	PCIE_J4_TXP10	GND	PCIE_J4_TXN12	GND	PCIE_J4_RXP12	GND
19	GND	PCIE_J4_TXN10	PCIE_J4_TXP11	GND	PCIE_J4_RXP10	PCIE_J4_RXN12	GND
18	GND	GND	PCIE_J4_TXN11	PCIE_J4_RXP8	PCIE_J4_RXN10	GND	GND
17	GND	PCIE_J4_TXP8	GND	PCIE_J4_RXN8	GND	PCIE_J4_RXP11	GND
16	GND	PCIE_J4_TXN8	PCIE_J4_TXP9	GND	PCIE_J4_RXP9	PCIE_J4_RXN11	GND
15	GND	GND	PCIE_J4_TXN9	GND	PCIE_J4__RXN9	GND	GND
12-14	GND	KEY AREA					
11	GND	SMB_CLK_PCH	PCIE_J4_TXP7	GND	PCIE_J4_RXP7	SMB_DATA_PCH	GND
10	GND	GND	PCIE_J4_TXN7	PCIE_X16_DP0	PCIE_J4_RXN7	GND	GND
9	GND	PCIE_J4_TXP5	GND	PCIE_X16_DN0	GND	PCIE_J4_RXP6	GND
8	GND	PCIE_J4_TXN5	PCIE_J4_TXP6	GND	PCIE_J4_RXP5	PCIE_J4_RXN6	GND
7	GND	GND	PCIE_J4_TXN6	PCIE_J4_RXP4	PCIE_J4_RXN5	GND	GND
6	GND	PCIE_J4_TXP2	GND	PCIE_J4_RXN4	GND	PCIE_J4_RXP3	GND
5	GND	PCIE_J4_TXN2	PCIE_J4_TXP3	GND	PCIE_J4_RXP2	PCIE_J4_RXN3	GND
4	GND	GND	PCIE_J4_TXN3	PCIE_J4_TXP4	PCIE_J4_RXN2	GND	GND
3	GND	PCIE_J4_RXP1	GND	PCIE_J4_TXN4	GND	PCIE_J4_TXP0	GND
2	GND	PCIE_J4_RXN1	PCIE_J4_RXP0	GND	PCIE_J4_TXP1	PCIE_J4_TXN0	GND
1	GND	GND	PCIE_J4_RXN0	GND	PCIE_J4_TXN1	GND	GND

Table 4-15: CompactPCI J4 Connector Pin Definition

CAUTION:

The J4 pin-out is assigned for PCIe x16. The J4 PCIe x16 pin assignment is not compatible with PICMG 2.5 R1.0 Computer Telephony Specification. Therefore, do not insert the cPCI-6940 into the peripheral slot of a PICMG 2.5 H.110 compliant backplane in order to avoid causing serious damage to the cPCI-6940.

CompactPCI J5 Connector

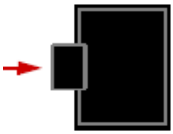
Pin	Z	A	B	C	D	E	F
22	GND	Power LED	LAN3_LED_ACT-L	NC	LAN4_LED_ACT-L	NC	GND
21	GND	USB3.0_TXAP	USB3.0_TXAN	GND	USB3.0_RXAP	USB3.0_RXAN	GND
20	GND	USB3.0_TXBP	USB3.0_TXBN	GND	USB3.0_RXBP	USB3.0_RXBN	GND
19	GND	SATA-RXP5	SATA-RXN5	GND	SATA-TXP5	SATA-TXN5	GND
18	GND	DVI2_CLK_P	DVI2_CLK_N	GND	GND	GND	GND
17	GND	DVI2_DATA1_P	DVI2_DATA1_N	GND	COM5_TX	COM5_RX	GND
16	GND	DVI2_SDA	DVI2_SCL	DVI2_HPD	GND	GND	GND
15	GND	DVI2_DATA2_P	DVI2_DATA2_N	GND	SATA-RXP2	SATA-RXN2	GND
14	GND	DVI2_DATA0_P	DVI2_DATA0_N	GND	SATA-TXP2	SATA-TXN2	GND
13	GND	LAN3_LED_100-L	LAN4_LED_100-L	NC	LAN4_LED_1G-L	LAN3_LED_1G-L	GND
12	GND	DVI1_SDA	DVI1_SCL	DVI1_HPD	NC	NC	GND
11	GND	DVI1_DATA2_P	DVI1_DATA2_N	GND	DVI1_CLK_P	DVI1_CLK_N	GND
10	GND	DVI1_DATA0_P	DVI1_DATA0_N	GND	DVI1_DATA1_P	DVI1_DATA1_N	GND
9	GND	GPIO1	GPIO2	GPIO3	GPIO4	GPIO5	GND
8	GND	HotSwap LED	WDTLED-L	GND	SATA-LED	NC	GND
7	GND	GND	GND	BAT-RTM	GND	GND	GND
6	GND	PCIE-CLK-DP1	PCIE-CLK-DN1	GND	PLTRST-L	NC	GND
5	GND	GND	GND	GND	GND	GND	GND
4	GND	PCIE-TXP3	PCIE-TXN3	GND	PCIE-RXP3	PCIE-RXN3	GND
3	GND	PCIE-TXP2	PCIE-TXN2	GND	PCIE-RXP2	PCIE-RXN2	GND
2	GND	PCIE-TXP1	PCIE-TXN1	GND	PCIE-RXP1	PCIE-RXN1	GND
1	GND	PCIE-TXP0	PCIE-TXN0	GND	PCIE-RXP0	PCIE-RXN0	GND

Table 4-16: CompactPCI J5 Connector Pin Definition

4.5 Switches and Buttons

System Reset Button (SW14)

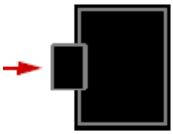
The cPCI-6940 has a system reset button on the faceplate. See “cPCI-6940 Series Board Layout - Solder Side” on page 20 and “cPCI-6940 Series Faceplate” on page 24 for the button location.



See “cPCI-6940 Series Board Layout” on page 19 for the following button and switch locations.

RTC Reset Button (SW13)

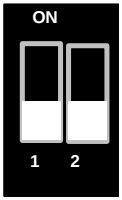
Press switch SW13 to reset the RTC and load default BIOS.



BIOS Protect (SW1)

SW1 is used to protect the BIOS from being written to. Changing SW1 settings will prevent the ME (Management Engine) from being overwritten or the BIOS settings from being changed or an upgrade applied. All are set to OFF by default.

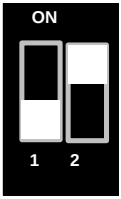
Pin	ON	OFF
1	ME protect	No ME protect (default)
2	BIOS protect	No BIOS protect (default)



VGA Output Settings (SW2)

Sets the VGA output to the port on the faceplate or rear I/O.

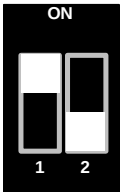
Pin	ON	OFF
1	VGA to rear	VGA to front (default)
2	NC	NC



Serial Port Setting (SW6)

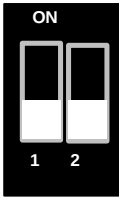
Sets the mode of the COM port on the faceplate.

Mode	1	2
RS-232 (default)	ON	OFF
RS-422	ON	ON
RS-485	OFF	ON



Debug Switches (SW11, SW12, SW_MOD1)

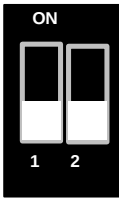
Switches SW11, SW12 and SW_MOD1 are for debugging purposes and should be left in the default settings (all OFF).



Mode Debug Switch (SW_MOD2)

Switch SW_MOD2 is for debugging purposes and should be left in the default settings (all OFF).

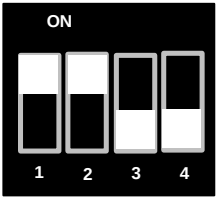
Pin#	Status	Description
1	ON	Force power on. The system will get power when the system is power up.
	OFF	IPMC power will control power input and scan devices before boot up (default).
2	ON	Reserved for debug
	OFF	Reserved for debug (default)



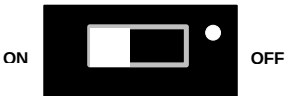
COM Debug Switches (SW_COMDEG1, SW_COMPW1)

Switch **SW_COMDEG1** is set 1, 2 ON and 3, 4 OFF by default to set the faceplate RJ-45 COM (CN12) serial port as a standard RS-232 serial port. The setting can be changed to use CN12 as an IPMI debugging port. Leave on default settings unless instructed by ADLINK.

SW_COMDEG1	Function
1, 2 ON, 3, 4 OFF	Normal COM (Default)
1, 2 OFF, 3, 4 ON	IPMI Debug



Switch **SW_COMPW1** is set ON by default. Leave on default settings unless instructed by ADLINK.



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5 Getting Started

This chapter describes the following installation procedures for the cPCI-6940.

- Memory module installation
- 2.5” SATA drive

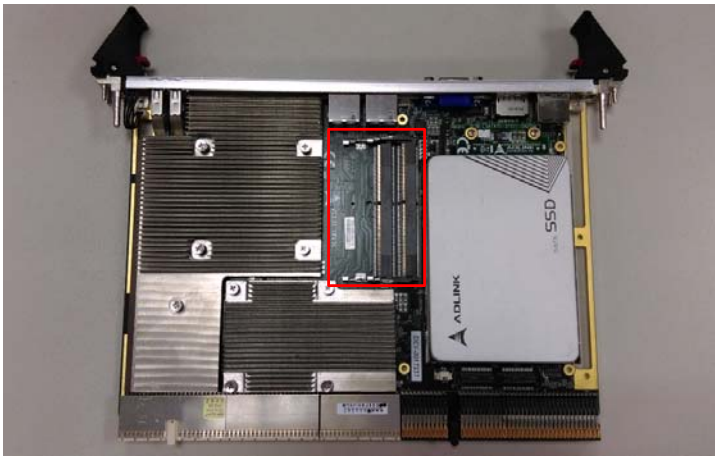
5.1 CPU and Heatsink

The cPCI-6940 Series come with CPU and heatsink pre-installed. Removal of heatsink/CPU by users is not recommended. Please contact your ADLINK service representative for assistance.

5.2 Memory Module Installation

The cPCI-6940 provides space to install two DRAM SODIMM memory modules. Follow the instructions below to install memory modules to the cPCI-6940.

1. Memory modules can be installed in the location marked below.



2. Insert the memory module into the memory slot, then push down on the DRAM module. Insert another DRAM module if required.

3. Completed memory installation.

NOTE:

If only one memory module is used, it must be installed in the upper memory slot (DIMM0).

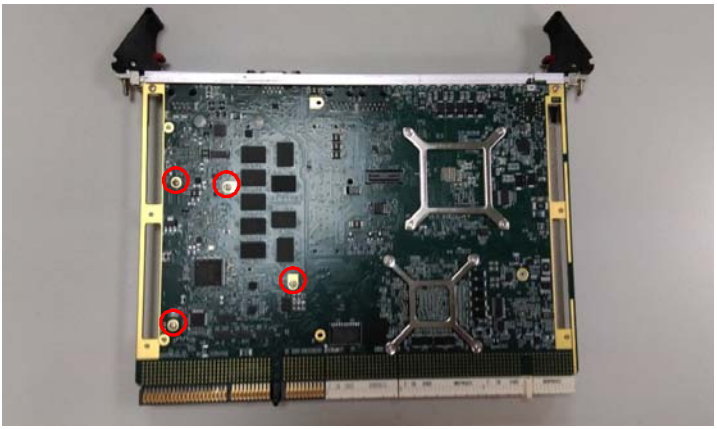
5.3 2.5" SATA Drive Installation

The cPCI-6940 provides space to install a 2.5” SATA drive.

1. Locate the DB-LSATA SATA adapter board, screws for assembling the 2.5" SATA drive and the HDD bracket in the accessory pack. Insert the 2.5" SATA drive into the SATA adapter board. Secure the drive to the bracket by fastening the four screws provided in the package in the locations marked below.

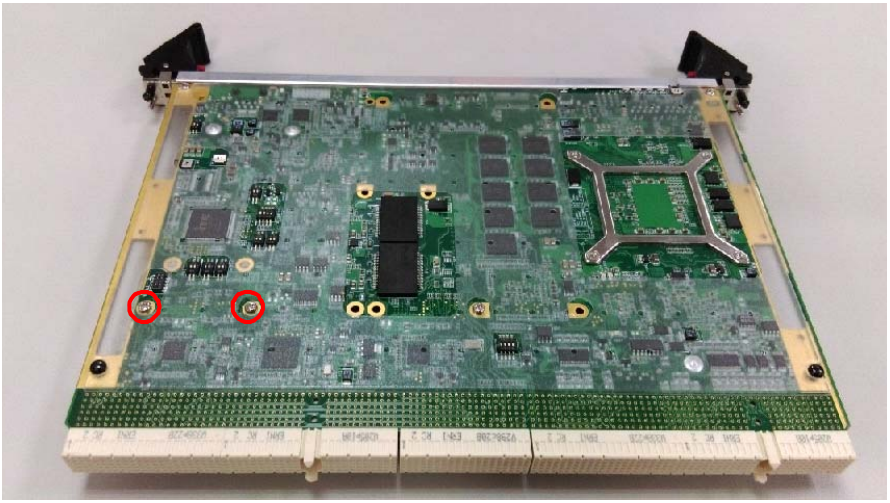
2. Connect the SATA adapter board to the cPCI-6940 and secure the drive bracket to DB-LSATA by securing two screws as circled below.

3. Turn the blade over and secure four screws as marked below.



4. Completed SATA drive installation.

5. Turn the blade over and secure with two screws as marked below to complete the SATA drive installation.



5.4 Installing the cPCI-6940 to the Chassis

The cPCI-6940 may be installed in a system or peripheral slot of a 6U CompactPCI chassis. These instructions are for reference only. Refer to the user guide that comes with the chassis for more information.

1. Be sure to select the correct slot depending on the operational purpose of the module. The system power may now be powered on or off.
2. Remove the blank face cover from the selected slot, if necessary.
3. Press down on the release catches of the cPCI-6940 ejector handles.
4. **Remove the black plastic caps securing the mounting screws to the faceplate.**
5. Align the module's top and bottom edges to the chassis card guides, and then carefully slide the module into the chassis. A slight resistance may be felt when inserting the module. If the resistance it too strong, check if there are bent pins on the backplane or if the board's connector pins are not properly aligned with connectors on the backplane. Then push the board until it is completely flush with the chassis.
6. Push the ejector handles outwards to secure the module in place, and then fasten the screws on the module faceplate.
7. Connect the cables and peripherals to the board, and then turn the chassis on if necessary.

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6 Driver Installation

The cPCI-6940 drivers can be downloaded from the ADLINK website (**http://www.adlinktech.com**). ADLINK provides validated drivers for Windows 7 and Windows Server 2012. We recommend using these drivers to ensure compatibility. The VxWorks BSP can be downloaded from the cPCI-6940 product page on the ADLINK website

6.1 cPCI-6940 Drivers

The following describes the cPCI-6940 driver installation procedures for Windows 7.

1. Install the Windows operating system before installing any driver. Most standard I/O device drivers are installed during Windows installation.
2. Install the **chipset driver** by extracting and running the program in **...\Chipset\Intel_Chipset_Win7x64_v10.1.2.10.zip**.
3. Install the **graphics driver** and utilities by extracting and running the program in **...\Graphics\AMD_Graphics_Win7x64_v15.7.1.zip**.
4. Install the **LAN drivers** by extracting and running the program in **…\LAN\Intel_LAN_Win7x64_v20.4.zip**.
5. Install the **Intel Rapid Storage Technology Utility** by extracting and running the program in **…\Intel_RST_Win7x64_v4.3.0.1223.zip**.
6. Install the USB 3.0 driver by extracting and running the program in **…\USB\Intel_USB30_Win7x64_v4.0.5.55.zip**.
7. Install the **audio driver** and utilities by extracting and running the program in **…\Audio\Realtek_High Definition Audio_Win7_32_6.0.1.6873.zip**.
8. **For cPCI-6940 8HP dual slot versions, the dual 10G ports require driver installation.** Install the 10G interface driver for 10G support by extracting and running the program in...**\Intel_10G LAN_Win7x64_v3.11.80.0.zip**.

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7 Utilities

7.1 Watchdog Timer

This section describes the operation of the cPCI-6940's watch dog timer (WDT). The primary function of the WDT is to monitor the cPCI-6940 operation and to reset the system if a software application fails to function as programmed. The following WDT functions may be controlled using a software application:

- enabling and disabling
- reloading timeout value

The cPCI-6940 custom WDT circuit is implemented using the internal IO of the ITE Super I/O IT8786 which is at 2Eh of LPC. The basic functions of the WDT include:

- Starting the timer countdown.
- Enabling or disabling WDT.
- Enable or disable WDT countdown LED ON.
- Reloading the timeout value to keep the watch dog from timing out.
- Setting the range of the timeout period from 1 to 15300 seconds.
- Sending a RESET signal to system when the watch dog times out

Using the Watchdog in an Application

The following section describes the WDT functions in an application. The WDT reset function is explained in the previous section. This can be controlled through the registers in the cPCI-6940 Super I/O.

An application using the reset feature enables the watchdog function, sets the count-down period, and reloads the timeout value periodically to keep it from resetting the system. If the timer countdown value is not reloaded, the watchdog resets the system hardware after its counter reaches zero.

For a detailed programming sample, refer to the sample code below.

WDT Sample Code

```
#include <stdio.h>
#include <stdlib.h>

typedefunsigned charBYTE;

void EnterConfig()
{
   outportb(SIO_CONFIG_INDEX, 0x87);
   outportb(SIO_CONFIG_INDEX, 0x01);
   outportb(SIO_CONFIG_INDEX, 0x55);
   outportb(SIO_CONFIG_INDEX, 0x55);
}

void ExitConfig()
{
   outportb(SIO_CONFIG_INDEX, 0x02);
   outportb(SIO_CONFIG_DATA, 0x02);
}

void LDNSelection(BYTE LDN)
{
   outportb(SIO_CONFIG_INDEX, 0x07);
   outportb(SIO_CONFIG_DATA, LDN);
}

void SIOBasicIORead(
   BYTE LDN,
   BYTE Register,
   BYTE *Data)
{
   LDNSelection(LDN);
   outportb(SIO_CONFIG_INDEX, Register);
   *Data = inportb(SIO_CONFIG_DATA);
}

void SIOBasicIOWrite(
   BYTE LDN,
   BYTE Register,
   BYTE Data)
{
```

```
   LDNSelection(LDN);
   outportb(SIO_CONFIG_INDEX, Register);
   outportb(SIO_CONFIG_DATA, Data);
}

BOOL StringToByte(char *string, BYTE *value)
{
   BYTE i, temp;
   *value = 0;
   for(i=0; string[i]!=NULL; ++i) {
        if(i>1) { printf("Digital count error!\n");
   return 0; }
        *value <<= 4;
        temp = toupper(string[i]);
        if(temp >='0' && temp <='9')
             *value += temp - '0';
        else if(temp >='A' && temp <='F')
             *value += temp - 'A' + 0x0a;
        else {
             printf("Input char[%c] is illegal!\n",
   string[i]);
             return 0;
        }
   }
   return1;
}

BOOL StringToWORD_Dec(char *string, WORD *value)
{
   BYTE i;
   WORD temp;

   *value = 0;
   for(i=0; string[i]!=NULL; ++i) {
        if(i>4) { printf("Digital count error!\n");
   return 0; }
        *value *= 10;
        temp = toupper(string[i]);
        if(temp >='0' && temp <='9')
             *value += temp - '0';
        else {
```

```
                printf("Input char[%c] is illegal!\n",
   string[i]);
                return 0;
           }
   }
   if(temp > 65535) {
           printf("Input number is large than
   65535!\n");
   }
   return1;
}

int IT8786_WatchDog(int argc, char *argv[])
{
   BYTE    bTemp, bUnit;
   WORD wWdtimer;

   printf("ADLINK WatchDog DOS Utility [Version
   1.00]\n\n");
   if((argc != 3) && strcmp(argv[1], "/?")) {
           printf("Invalid command, please type /? to
   get the details.\n");
           return 0;
   }
   if(!strcmp(argv[1], "/?")) {
           printf("WatchDog [argument1]
   [argument2]\n\n");
           printf("argument1 :\n");
           printf("   1 - Second\n");
           printf("   0 - Minute\n");
           printf("argument2 :\n");
           printf("   Time-out value\n\n");
           printf("Example below for 10 seconds.\n");
           printf("   WatchDog 1 10\n");
           printf("Example below for 3 minutes.\n");
           printf("   WatchDog 0 3\n");
           return 0;
   }

   StringToByte(argv[1], &bUnit);
   if((bUnit != 0) && (bUnit != 1)) {
```

```
        printf("Argument1 is a invalid
    number[%d].\n", bUnit);
        return 1;
    }

    StringToWORD_Dec(argv[2], &wWdtimer);

    EnterConfig();

// Implement  Watch Dog
    SIOBasicIORead(0x07, 0x29, &bTemp);
    bTemp &= ~BIT6; // default function = KRST
    SIOBasicIOWrite(0x07, 0x29, bTemp);

// Config settings
    if(bUnit) {
        bTemp = 0xd0; // second
    } else {
        bTemp = 0x50; // minute
    }
    SIOBasicIOWrite(0x07, 0x72, bTemp);

// Set timer value
    SIOBasicIOWrite(0x07, 0x74,
    (BYTE)(wWdtimer>>8));
    SIOBasicIOWrite(0x07, 0x73, (BYTE)wWdtimer);

// Program led blinking
    SIOBasicIORead(0x07, 0x25, &bTemp);
    bTemp |= BIT2;
    SIOBasicIOWrite(0x07, 0x25, bTemp);

    SIOBasicIOWrite(0x07, 0xF8, 0x0A);

    ExitConfig();

    return 0;
}
```

7.2 User LED Programming

The eight User LEDs on the front panel display port 80h POST codes in hexadecimal during boot up. Users can use the POST codes to identify issues during the BIOS POST process. In default mode, these eight LEDs display the POST code output to Port 80h during system bootup (see “User LEDs” on page 26).

After the system is under OS control, the eight User LEDs can be controlled as user defined LEDs. The LEDs are connected to eight GPIO pins of the Super I/O IT8786. Users can follow the sample code below to control the LEDs.

User LED Sample Code

```
#define IT8786_GPIO_BASE_ADDRESS 0xa00
typedef unsigned char BYTE;

//================================================
//
// Procedure: LedCheckpoint
//
//================================================
VOID LedCheckpoint(IN BYTE Checkpoint)
{
   BYTE bData = 0xFF, i;

   for(i=0; i<8; i++) {
        if(Checkpoint&(1<<i))
             bData &= ~(UINT8)(1<<i);
   }

   outportb(IT8786_GPIO_BASE_ADDRESS+0x06, bData);
}
```

8 BIOS Setup Utility

The following chapter describes basic navigation for the AMI EFI BIOS setup utility.

8.1 Starting the BIOS

To enter the setup screen, follow these steps:

1. Power on the motherboard
2. Press the < Delete > key on your keyboard when you see the following text prompt:
   < Press DEL to run Setup >
3. After you press the < Delete > key, the main BIOS setup menu displays. You can access the other setup screens from the main BIOS setup menu.

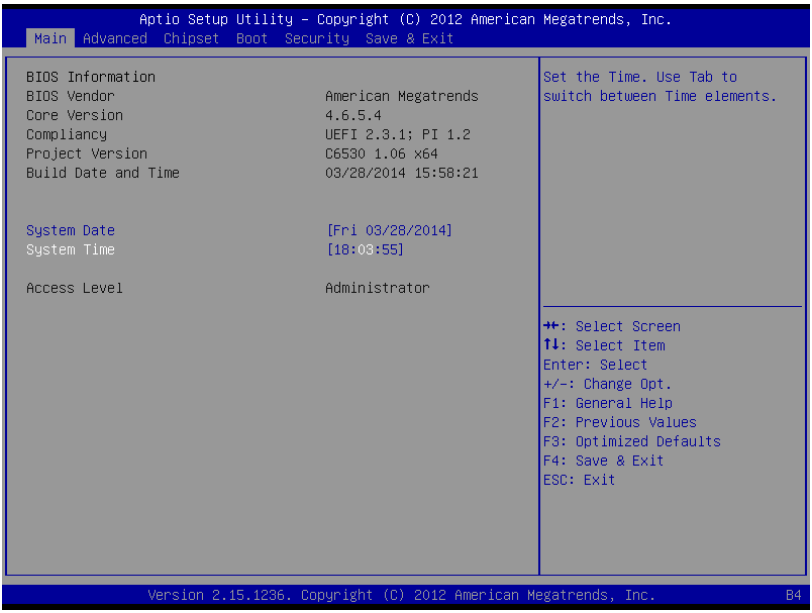
Note: In most cases, the < Delete > key is used to invoke the setup screen. There are several cases that use other keys, such as < F1 >, < F2 >, and so on.

Setup Menu

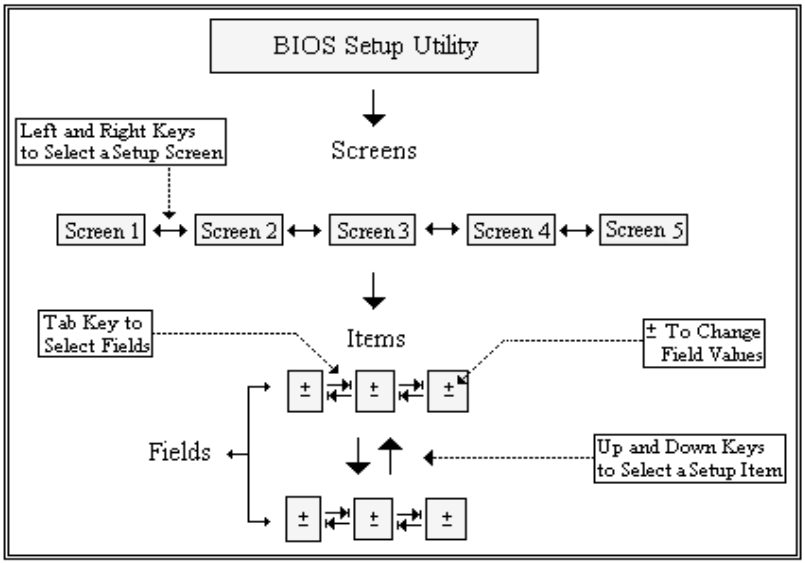
The main BIOS setup menu is the first screen that you can navigate. Each main BIOS setup menu option is described in this user's guide.

The Main BIOS setup menu screen has two main frames. The left frame displays all the options that can be configured. "Grayed" options cannot be configured, "Blue" options can be.

The right frame displays the key legend. Above the key legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white. Often a text message will accompany it.



Navigation



Note: There is a hot key legend located in the right frame on most setup screens.

Keyboard Commands

< > The *Left* and *Right* "Arrow" keys allow you to select a setup screen.

^ v The *Up* and *Down* "Arrow" keys allow you to select a setup screen.

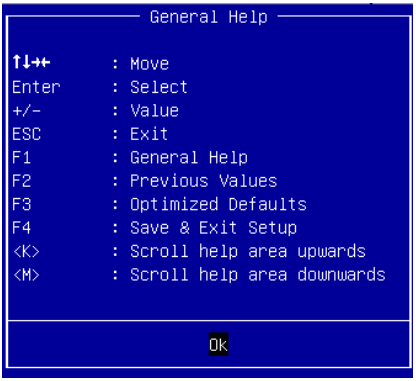
+ - The *Plus* and *Minus* keys allow you to change the field value of a particular setup item.

Tab Moves the cursor to the next configurable item or to the next field.

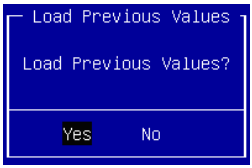
Hotkey Descriptions

Enter The < Enter > key allows you to display or change the setup option listed for a particular setup item. The < Enter > key can also allow you to display the setup sub-screens.

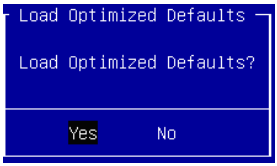
F1 The < F1 > key allows you to display the General Help screen. Press the < F1 > key to open the General Help screen.



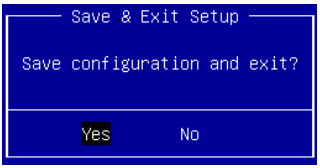
F2 The < F2 > key on your keyboard is the previous values key. It is not displayed on the key legend by default. To set the previous values settings of the BIOS, press the < F2 > key on your keyboard. It is located on the upper row of a standard 101 keyboard. The previous values settings allow the motherboard to boot up with the least amount of options set. This can lessen the probability of conflicting settings.



F3 The < F3 > key on your keyboard is the optimized defaults key. To set the optimized defaults settings of the BIOS, press the < F3 > key on your keyboard. It is located on the upper row of a standard 101 keyboard. The optimized defaults settings allow the motherboard to boot up with the optimized defaults of options set. This can lessen the probability of conflicting settings.

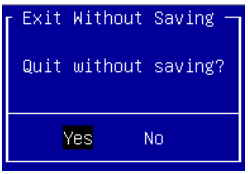


F4 The < F4 > key allows you to save any changes you have made and exit Setup. Press the < F10 > key to save your changes. The following screen will appear:



Press the < Enter > key to save the configuration and exit. You can also use the < Arrow > key to select Cancel and then press the < Enter > key to abort this function and return to the previous screen.

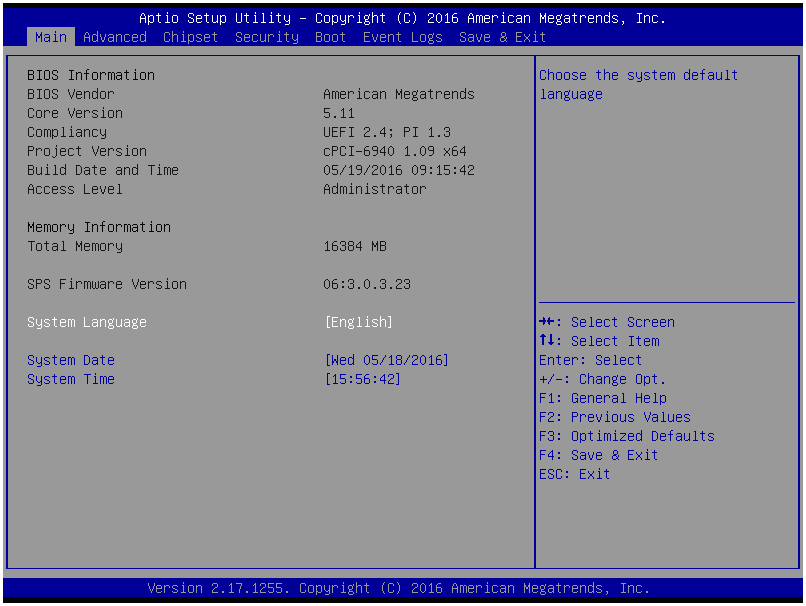
ESC The < Esc > key allows you to discard any changes you have made and exit the Setup. Press the < Esc > key to exit the setup without saving your changes. The following screen will appear:



Press the < Enter > key to discard changes and exit. You can also use the < Arrow > key to select Cancel and then press the < Enter > key to abort this function and return to the previous screen.

8.2 Main Setup

When you first enter the Setup Utility, you will enter the Main setup screen. You can always return to the Main setup screen by selecting the Main tab. There are two Main Setup options. They are described in this section. The Main BIOS Setup screen is shown below.



System & Board Info

BIOS Vendor

Displays the BIOS vendor.

Core Version

Displays the BIOS core version.

Project Version

Displays the current BIOS revision.

Build Data and Time

Displays the BIOS build data.

Total Memory

Displays the platform total memory size.

SPS Firmware Version

Displays the platform SPS firmware version.

System Time/System Date

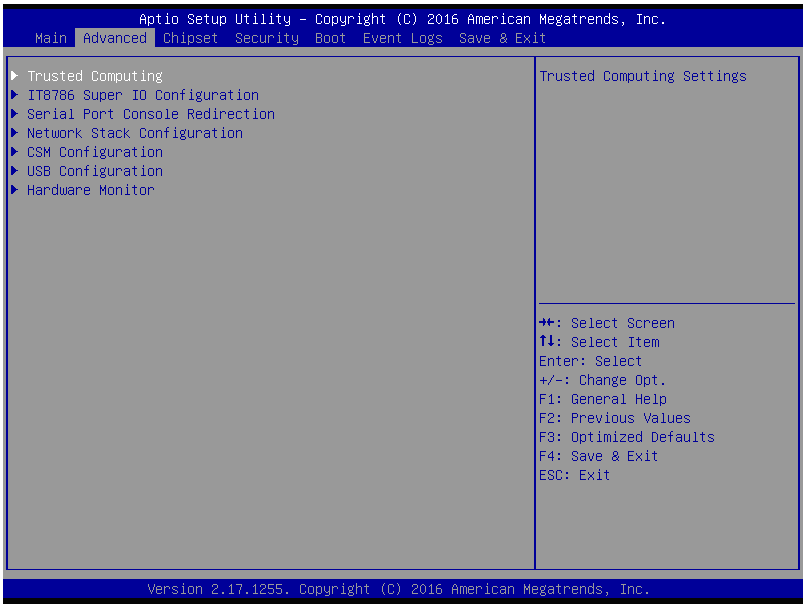
Use this option to change the system time and date. Highlight System Time or System Date using the < Arrow > keys. Enter new values using the keyboard. Press the < Tab > key or the < Arrow > keys to move between fields. The date must be entered in MM/DD/YY format. The time is entered in HH:MM:SS format.

Note: The time is in 24-hour format. For example, 5:30 A.M. appears as 05:30:00, and 5:30 P.M. as 17:30:00.

8.3 Advanced BIOS Setup

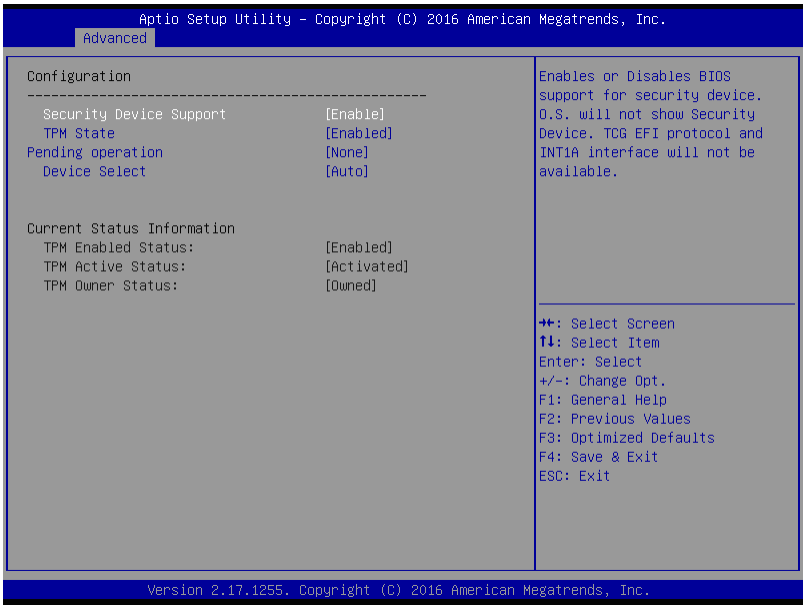
Select the Advanced tab from the setup screen to enter the Advanced BIOS Setup screen. You can select any of the items in the left frame of the screen to go to the sub menu for that item. You can display an Advanced BIOS Setup option by highlighting it using the < Arrow > keys. The Advanced BIOS Setup screen is shown below.

The sub menus are described on the following pages.



8.3.1 Trusted Computing

Trusted Computing is an industry standard to make personal computers more secure through a dedicated hardware chip, called a Trusted Platform Module (TPM). This option allows you to enable or disable the TPM support.



Security Device Support

OS will not show TPM. Reset of platform is required. Set this value to Enabled/Disabled.

TPM State

Determine whether TPM state change requires Password Authentication. Set this value to Enabled/Disabled.

Pending TPM operation

Schedule TPM operation. The settings for this value are Enable, Disable and Clear.

Device Select

TPM 1.2 will restrict support to TPM 1.2 devices, TPM 2.0 will restrict support to TPM 2.0 devices, Auto will support both with the default set to TPM 2.0 devices if not found, TPM 1.2 devices will be enumerated

TPM Enabled Status

Displays TPM enabled status.

TPM Active Status

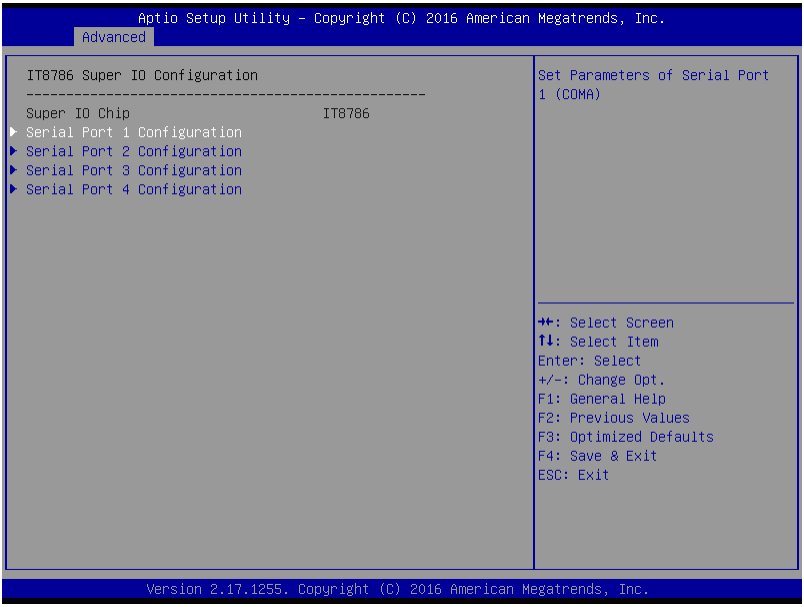
Displays TPM active status.

TPM Owner Status

Displays TPM owner status.

8.3.2 IT8786 Super IO Configuration

You can use this screen to select options for the IT8786 Super IO Configuration Settings. Use the up and down < Arrow > keys to select an item. Use the < + > and < - > keys to change the value of the selected option. A description of the selected item appears on the right side of the screen. The settings are described on the following pages. An example of the IT8786 Super IO Configuration screen is shown below.

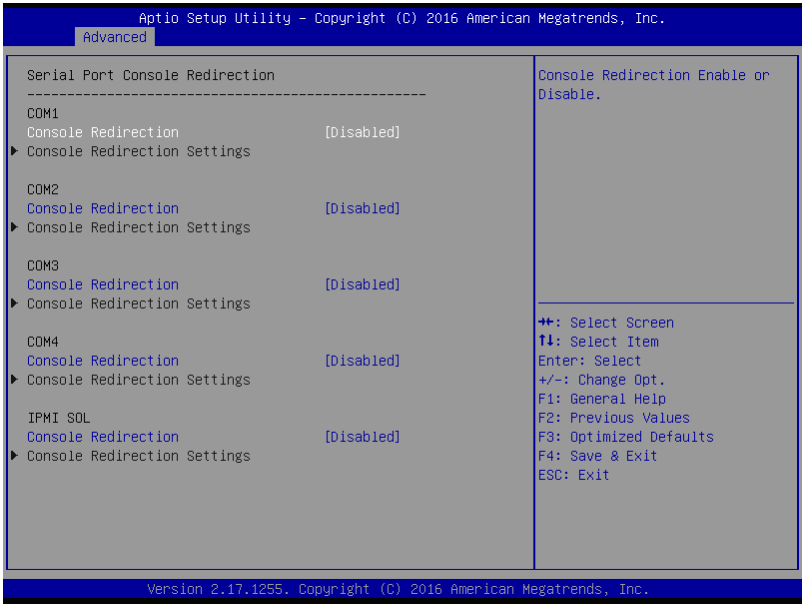


Serial Port 1-4 Configuration

Setttings for serial ports 1-4.

8.3.3 Console Redirection

You can use this screen to select options for the serial port console redirection settings. Use the up and down < Arrow > keys to select an item. Use the < + > and < - > keys to change the value of the selected option. A description of the selected item appears on the right side of the screen. The settings are described on the following pages. An example of the Serial Port Console Redirection screen is shown below.

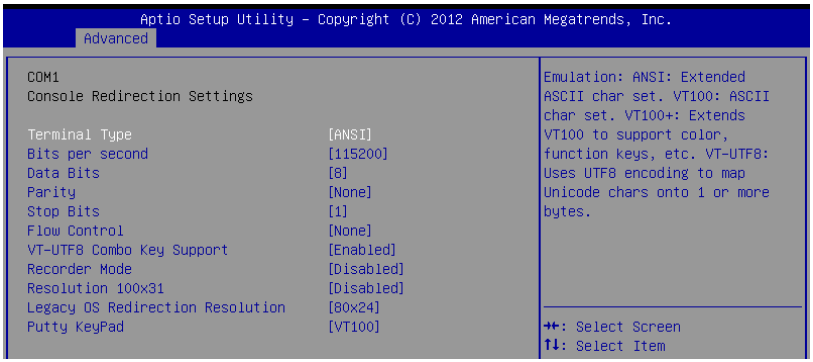


Console Redirection

Set this value to Enabled/Disabled.

Console Redirection Settings

The settings specify how the host computer and the remote computer will exchange data. Both computers should have the same or compatible settings. The screen is shown below.



Terminal Type

VT100+ is the preferred terminal type for out-of-band management. Configuration options: VT100, VT100+, VT-UTF8, ANSI.

Bits per second

Select the bits per second you want the serial port to use for console redirection. The options are 115200, 57600, 38400, 19200, 9600.

Data Bits

Select the data bits you want the serial port to use for console redirection. Set this value to 7, 8.

Parity

Set this option to select Parity for console redirection. The settings for this value are None, Even, Odd, Mark, Space.

Stop Bits

Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit. Set this value to 1 and 2.

Flow Control

Set this option to select Flow Control for console redirection. The settings for this value are None, Hardware RTS/CTS.

VT-UTF8 Combo Key Support

Enables VT-UTF8 combination key support for ANSI/VT100 terminals.Set this value to Enabled/Disabled.

Recorder Mode

When this mode is enabled, only text will be sent. This is to capture terminal data. Set this value to Enabled/Disabled.

Resolution 100x31

Set this option to extended terminal resolution. Set this value to Enabled/Disabled.

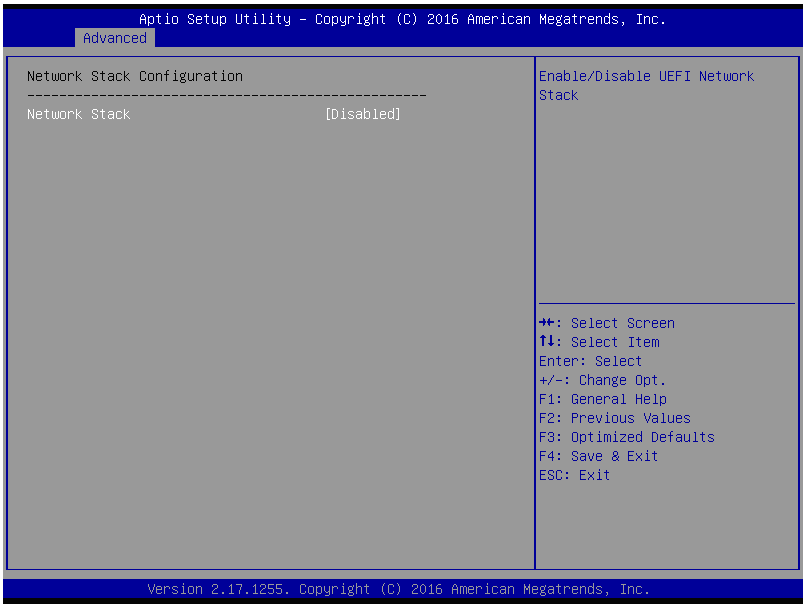
Legacy OS Redirection

On legacy OS, the number of rows and columns supported for redirection. Set this value to 80x24, 80x25.

Putty Key Pad

Select FunctionKey and KeyPad on Putty. Set this value to VT100, LINUX, XTERMR6, SCO, ESCN, VT400.

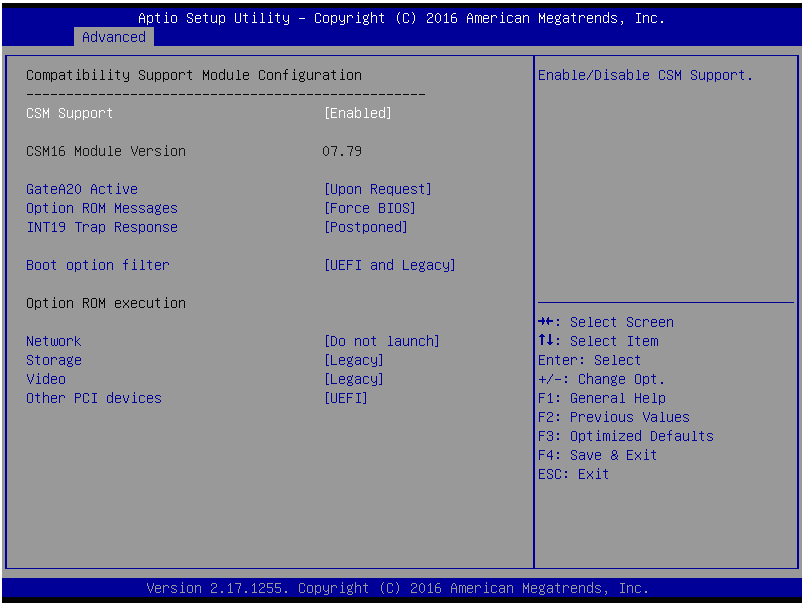
8.3.4 Network Stack Configuration



Network Stack

Enable/Disable UEFI Network Stack.

8.3.5 CSM Configuration



CSM Support

Enable/Disable CSM Support.

GateA20 Active

Upon Request: GA20 can be disabled using BIOS services. Always: do not allow disabling of GA20; this option is useful when any RT code is executed above 1MB.

Option ROM Messages

Set the display mode for Option ROM.

Int19 Trap Response

BIOS reaction on INT19 trapping by Option ROM: IMMEDIATE - execute the trap right away; POSTPONED - execute the trap during legacy boot.

Boot Option Filter

This option controls Legacy/UEFI ROM priority. Set this value to UEFI and Legacy, Legacy only, UEFI only.

Network

Controls the execution of UEFI and Legacy PXE OpROM. Set this value to Do not launch, Legacy, UEFI.

Storage

Controls the execution of UEFI and Legacy PXE OpROM. Set this value to Do not launch, Legacy, UEFI.

Video

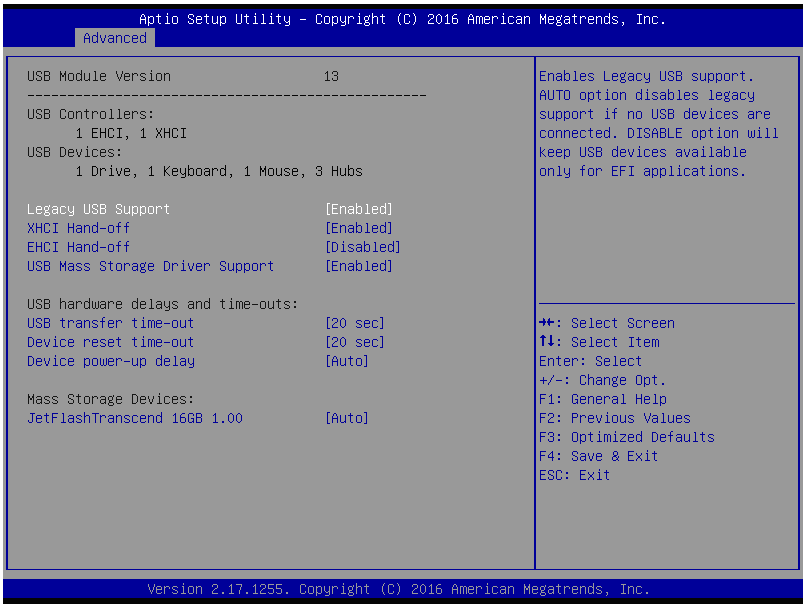
Controls the execution of UEFI and Legacy PXE OpROM. Set this value to Do not launch, Legacy, UEFI.

Other PCI Devices

Determines OpROM execution policy for devices other than Network, Storage, or Video. Set this value to Disable, Legacy, UEFI.

8.3.6 USB Configuration

You can use this screen to select options for the USB Configuration. Use the up and down < Arrow > keys to select an item. The screen is shown below.



Legacy USB Support

Enables legacy USB support. Auto option disables legacy support if no USB devices are connected. Disable option will keep USB devices available only for EFI applications. Set this value to Enabled/Disabled/Auto.

XHCI Hand-off

This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.

EHCI Hand-off

This is a workaround for OSes without EHCI hand-off support. The EHCI ownership change should be claimed by EHCI driver.

USB Mass Storage Driver Support

Enable/Disable USB Mass Storage Driver Support.

USB Transfer Time-out

The time-out value for Control, Bulk and Interrupt transfers.

Device Reset Time-out

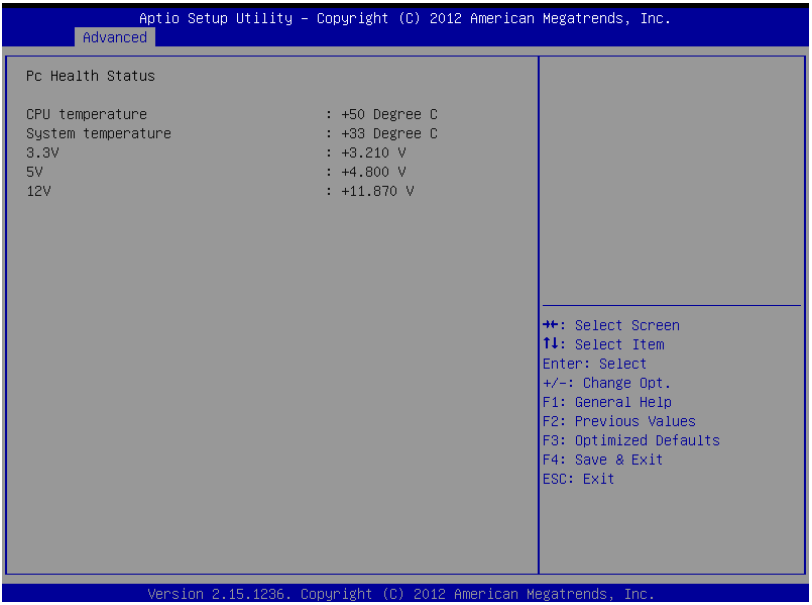
USB mass storage device Start Unit command time-out.

Device Power-up Delay

Maximum time the device will take before it properly reports itself to the Host Controller. 'Auto' uses default value: for a Root port it is 100 ms, for a Hub port the delay is taken from Hub descriptor.

8.3.7 Hardware Monitor

This option displays the current status of all of the monitored hardware devices/components such as voltages and temperatures.



CPU Temperature

Displays current CPU temperature.

System Temperature

Displays current system temperature.

3.3V

Displays current system 3.3V voltage.

5V

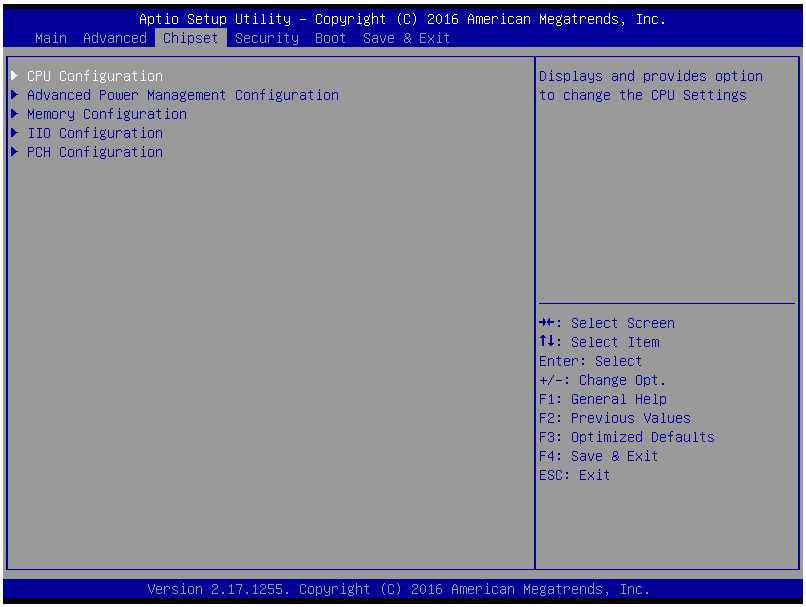
Displays current system 5V voltage.

12V

Displays current system 12V voltage.

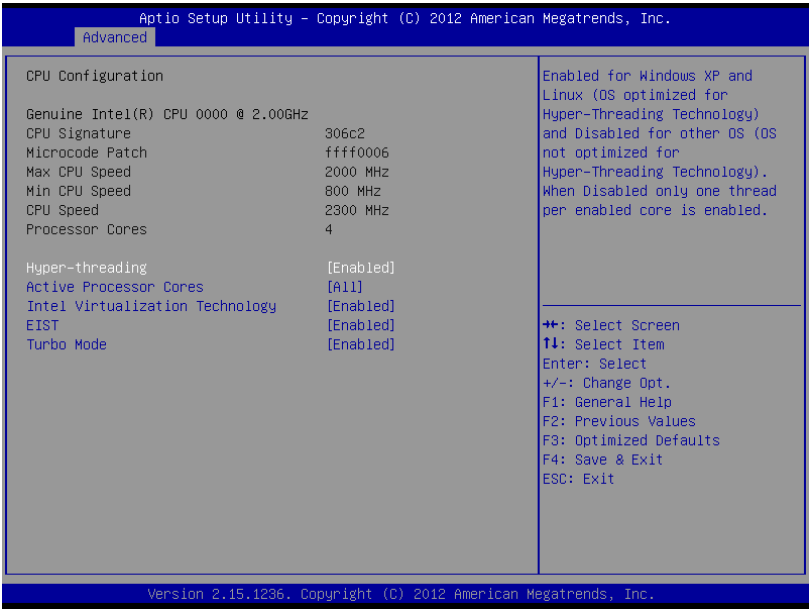
8.4 Chipset Setup

Select the Chipset tab from the setup screen to enter the Chipset BIOS Setup screen. You can select any of Chipset BIOS Setup options by highlighting it using the < Arrow > keys. The Chipset BIOS Setup screen is shown below.



8.4.1 CPU Configuration

You can use this screen to select options for the CPU Configuration Settings. Use the up and down < Arrow > keys to select an item. Use the < + > and < - > keys to change the value of the selected option. A description of the selected item appears on the right side of the screen. The settings are described on the following pages. An example of the CPU Configuration screen is shown below.



Core Enabled

Number of cores to enable. 0 means all cores.

Hyper-Threading [ALL]

Enables Hyper Threading(Software Method to Enable/Disable Logical Processor threads).

Execute Disable Bit

When disabled, forces the XD feature flag to always return 0.

Enable Intel TXT Support

Enables Intel Trusted Execution Technology Configuration.

VMX

Enables the Vanderpool Technology, takes effect after reboot.

Enable SMX

Enables Safer Mode Extensions.

Hardware Prefetcher

MLC Streamer Prefetcher (MSR 1A4h Bit[0])

Adjacent Cache Prefetch

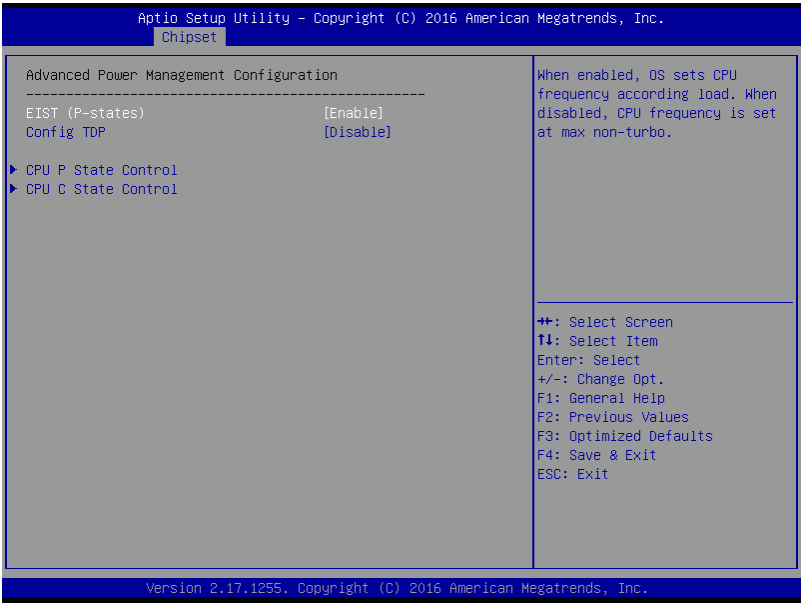
MLC Spatial Prefetcher (MSR 1A4h Bit[1])

X2APIC

Enable/Disable extended APIC support.

8.4.2 Advanced Power Management Configuration

You can use this screen to select options for the Advanced Power Management Configuration Settings. Use the up and down < Arrow > keys to select an item. Use the < + > and < - > keys to change the value of the selected option. A description of the selected item appears on the right side of the screen. The settings are described on the following pages. An example of the Advanced Power Management Configuration screen is shown below.



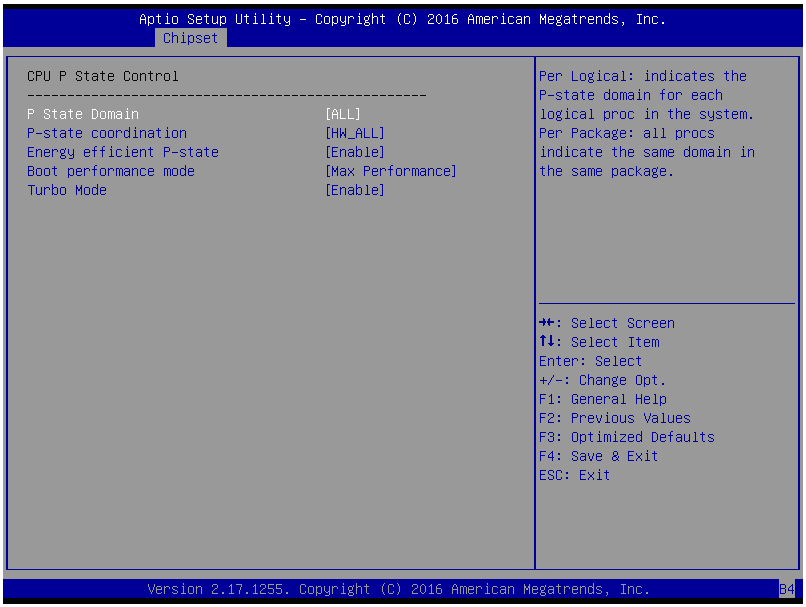
EIST (P-states)

When enabled, OS sets CPU frequency according to load. When disabled, CPU frequency is set at max non-Turbo.

Config TDP

Option to disable/enable Config TDP.

CPU P State Control



P State Domain

Per Logical: indicates the P-state domain for each logical proc in the system. Per Package: all procs indicate the same domain in the same package.

P-state Coordination

HW_ALL (hardware) coordination is recommended over SW_ALL and SW_ANY (software coordination).

Energy Efficient P-state

Enable/Disable Energy efficient P-state feature. When set to 0, will disable access to ENERGY_PERFORMANCE_BIAS MSR and CPUID Function 6 EAX[3] will read 0 indicating nosupport for Energy Efficient policy setting. When set to 1 will enable access to ENERGY_PERFORMANCE_BIAS MSR 1B0h and CPUID Function 6 EAX[3] will read 1 indicating Energy Efficient Policy setting is supported.

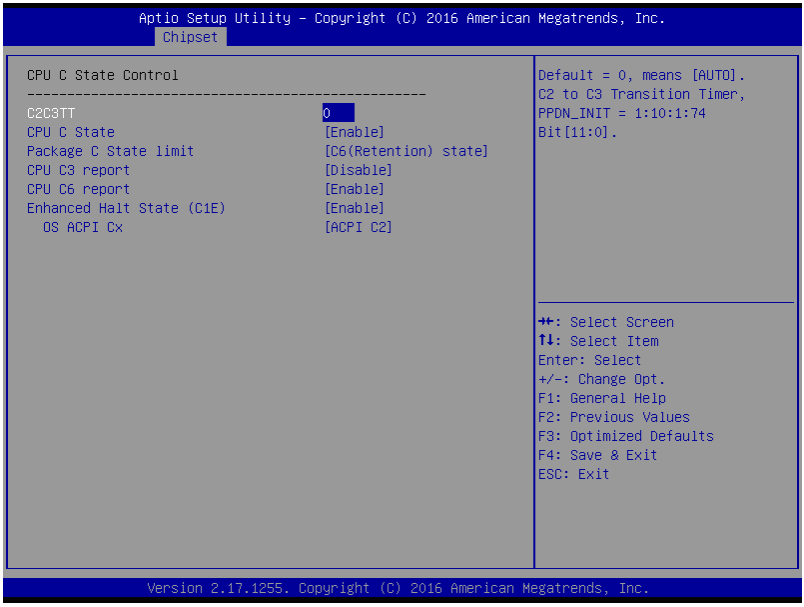
Boot Performance Mode

Select the performance state that the BIOS will set before OS handoff.

Turbo Mode

Enable or Disable CPU Turbo mode.

CPU C State Control



C2C3TT

Default = 0, means [AUTO]. C2 to C3 Transition Timer, PPDN_INIT = 1:10:1:74 Bit[11:0].

CPU C State

Enables the Enhanced Cx state of the CPU. Takes effect after reboot.

Package C State Limit

Select Package C State limit.

CPU C3 Report

Enable/Disable CPU C3 (ACPI C2) report to OS. Recommended to be disabled.

CPU C6 Report

Enable/Disable CPU C6 (ACPI C2) report to OS Recommended to be enabled.

Enhanced Halt State (C1E)

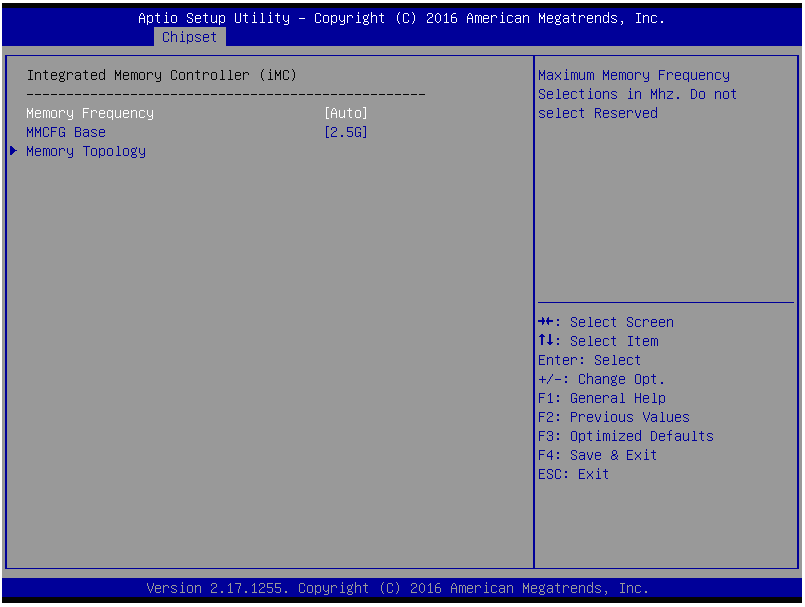
Enables the Enhanced C1E state of the CPU. Takes effect after reboot.

OS ACPI Cx

Report CC3/CC6 to OS ACPI C2 or ACPI C3.

8.4.3 Memory Configuration

You can use this screen to select options for the Memory Configuration Settings. Use the up and down < Arrow > keys to select an item. Use the < + > and < - > keys to change the value of the selected option. A description of the selected item appears on the right side of the screen. The settings are described on the following pages. An example of the Memory Configuration screen is shown below.



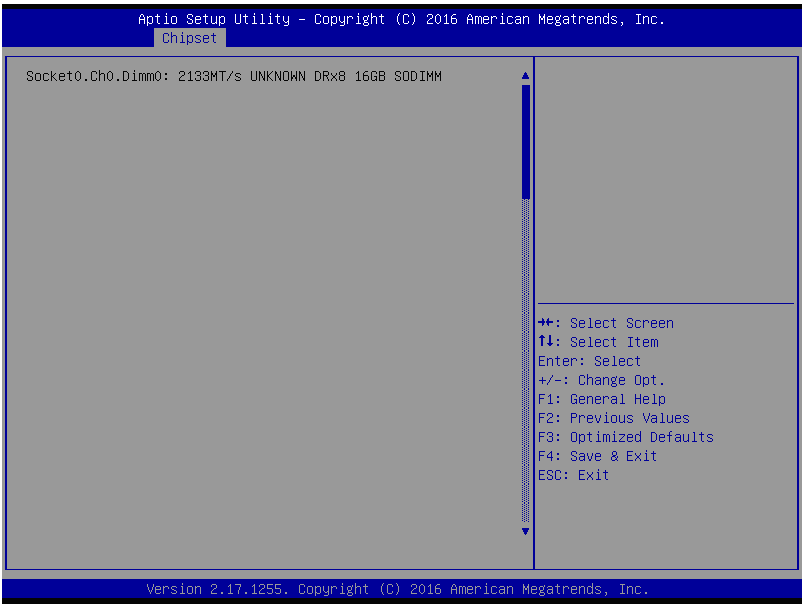
Memory Frequency

Maximum Memory Frequency Selections in MHz. Do not select Reserved.

MMCFG Base

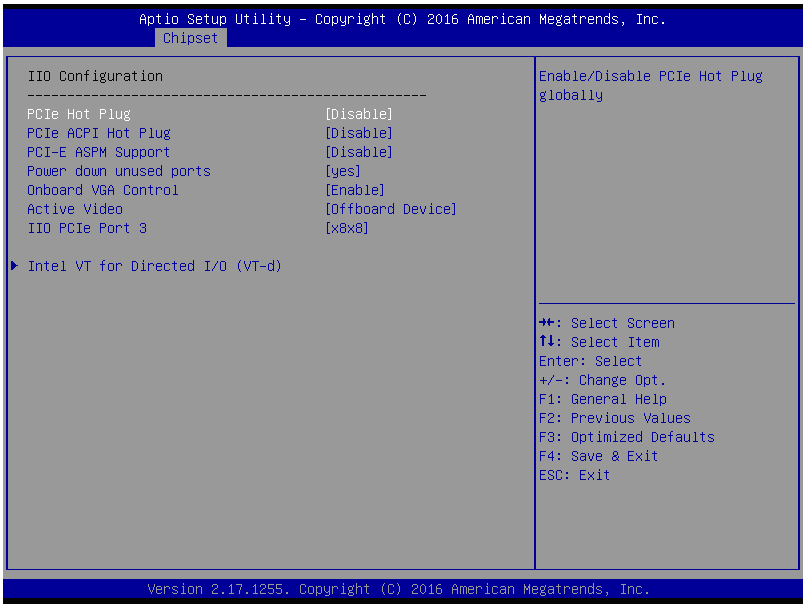
Select MMCFG Base.

Memory Topology



8.4.4 IIO Configuration

You can use this screen to select options for the Integrated I/O (IIO) Configuration Settings. Use the up and down < Arrow > keys to select an item. Use the < + > and < - > keys to change the value of the selected option. A description of the selected item appears on the right side of the screen. The settings are described on the following pages. An example of the IIO Configuration screen is shown below.



PCIe Hot Plug

Enable/Disable PCIe Hot Plug globally.

PCIe ACPI Hot Plug

Enable/Disable PCIe ACPI Hot Plug globally, or allow per-port control. When Disabled, MSI is generated on HP event. When Enabled, _HPGPE message is generated.

PCI-E ASPM Support

This option enables/disables the ASPM support for all down-stream devices.

Power Down Unused Ports

Power down unused ports.

Onboard VGA Control

Enable/Disable onboard VGA.

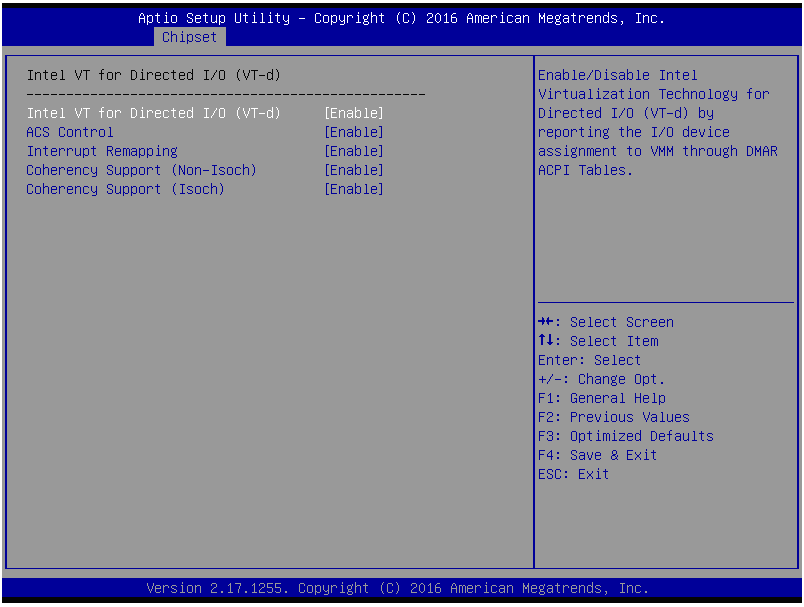
Active Video

Select active Video type.

IIO PCIe Port 3

Selects PCIe port bifurcation for PCIe x16 to J4 connector and XMC slot. Options: **x16** (PCIe x16 to J4), **x8x8** (PCIe x8 to J4, x8 to XMC).

Intel VT for Directed I/O (VT-d)



Intel VT for Directed I/O (VT-d)

Enable/Disable Intel Virtualization Technology for Directed I/O (VT-d) by reporting the I/O device assignment to VMM through DMAR ACPI Tables.

ACS Control

Enable: Programs ACS only to Chipset PCIe Root Ports Bridges; Disable: Programs ACS to all PCIe bridges.

Interrupt Remapping

Enable/Disable VT_D Interrupt Remapping Support.

Coherency Support (Non-Isoch)

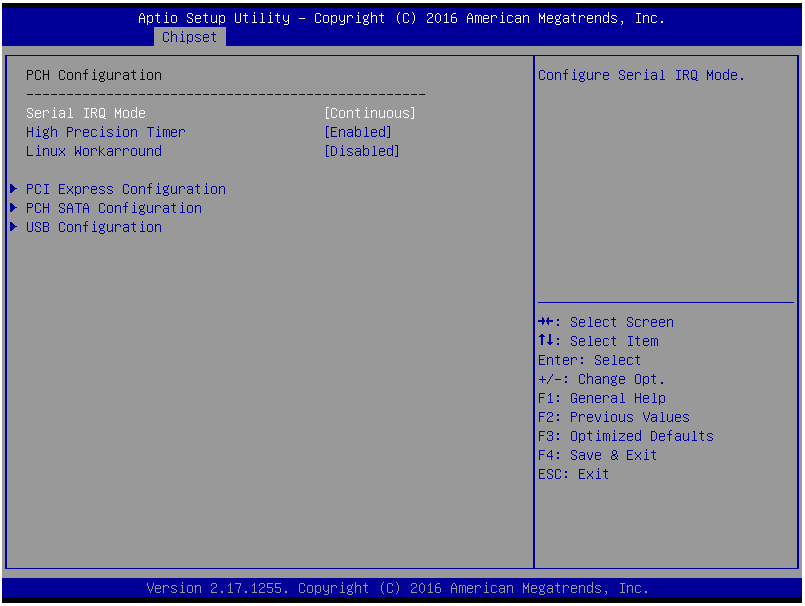
Enable/Disable Non-Isoch VT_D Engine Coherency support.

Coherency Support (Isoch)

Enable/Disable Isoch VT_D Engine Coherency support.

8.4.5 PCH Configuration

You can use this screen to select options for the PCH Configuration Settings. Use the up and down < Arrow > keys to select an item. Use the < + > and < - > keys to change the value of the selected option. A description of the selected item appears on the right side of the screen. The settings are described on the following pages. An example of the PCH Configuration screen is shown below.



Serial IRQ Mode

Configure Serial IRQ Mode.

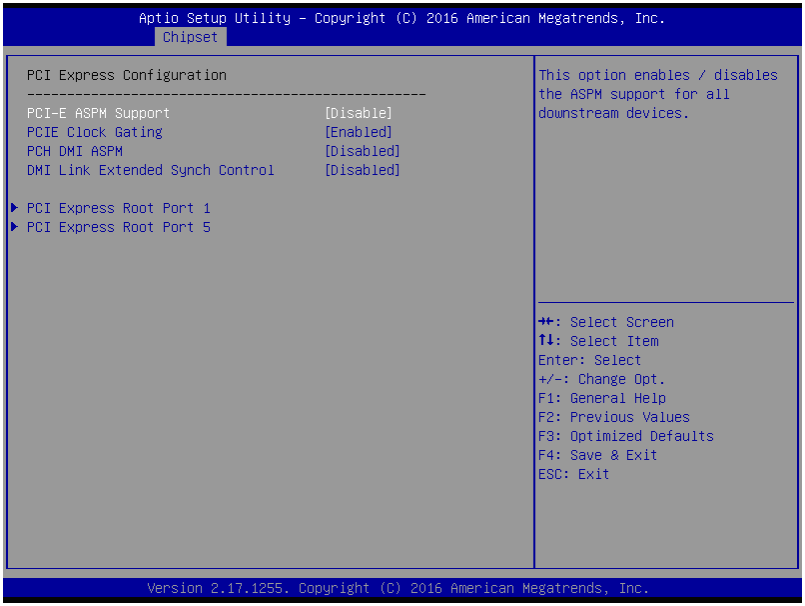
High Precision Timer

Enable or Disable the High Precision Event Timer.

Linux Workaround

Enable or Disable Linux workaround.

PCI Express Configuration



PCI-E ASPM Support

This option enables/disables the ASPM support for all downstream devices.

PCIE Clock Gating

PCIE Clock Gating Enable/Disable for all PCH PCIE Ports.

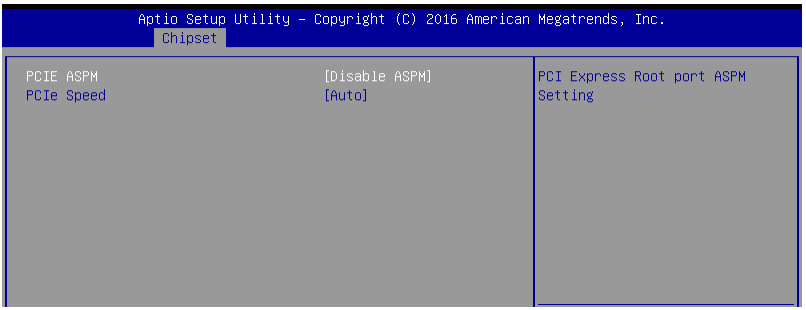
PCH DMI ASPM

PCH DMI ASPM setting.

DMI Link Extended Synch Control

The control of Extended Synch on SB side of the DMI Link.

PCI Express Root Port 1



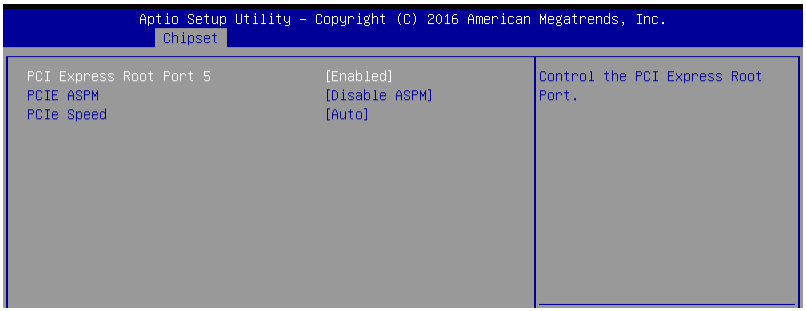
PCIE ASPM

PCI Express Root port ASPM Setting.

PCIe Speed

Configure PCIe Speed.

PCI Express Root Port 5



PCI Express Root Port 5

Control the PCI Express Root Port.

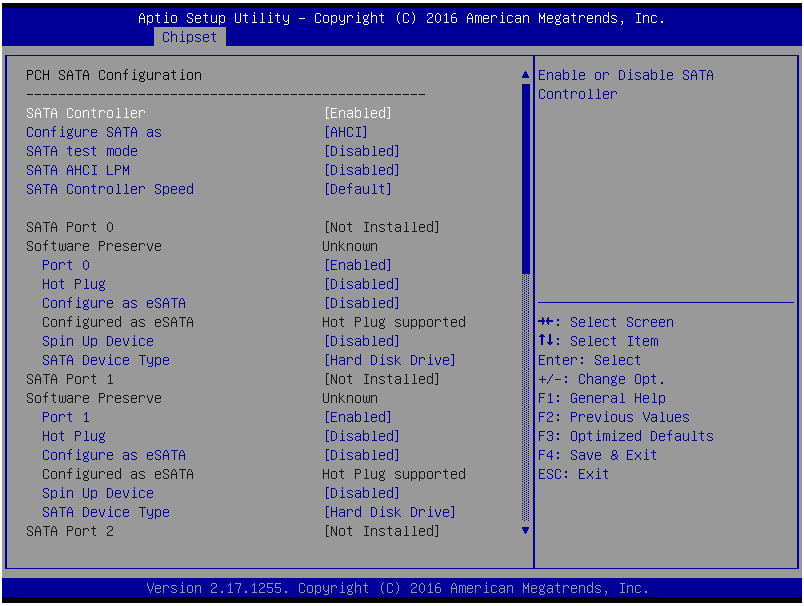
PCIE ASPM

PCI Express Root port ASPM Setting.

PCIe Speed

Configure PCIe Speed.

PCH SATA Configuration



SATA Controller

Enable or Disable SATA controller.

Configure SATA as

This will configure SATA as IDE, RAID or AHCI.

SATA Test Mode

Enable/Disable SATA test mode.

SATA AHCI LPM

Enables/Disables Link Power Management.

SATA Controller Speed

Indicates the maximum speed the SATA controller can support.

Port N

Enable or Disable SATA port.

Hot Plug

Designates this port as Hot Pluggable.

Configure as eSATA

Configures port as external SATA (eSATA).

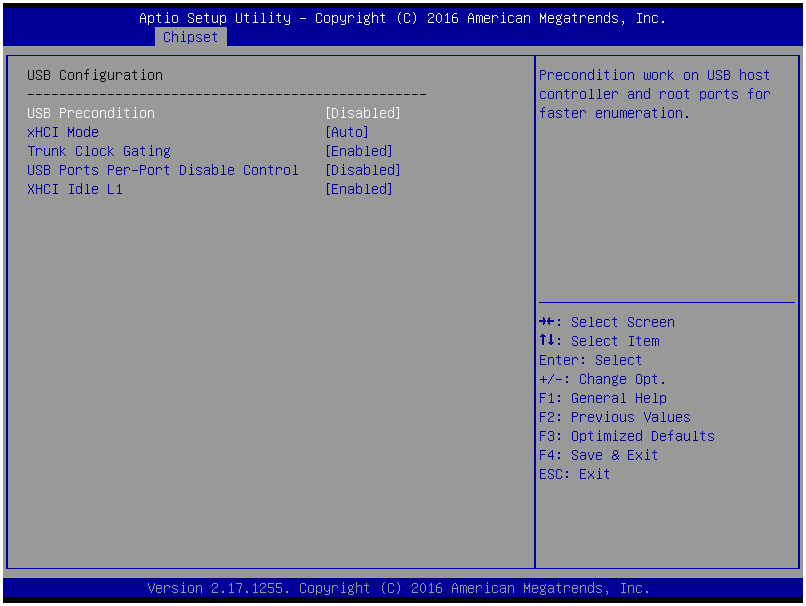
Spin Up Device

If enabled for any of ports Staggered Spin Up will be performed and only the drives which have this option enabled will spin up at boot. Otherwise all drives spin up at boot.

SATA Device Type

Identify the SATA port is connected to Solid State Drive or Hard Disk Drive.

USB Configuration



USB Precondition

Precondition work on USB host controller and root ports for faster enumeration.

xHCI Mode

Mode of operation of xHCI controller.

Trunk Clock Gating

Enable/Disable BTCG.

USB Ports Per-Port Disable Control

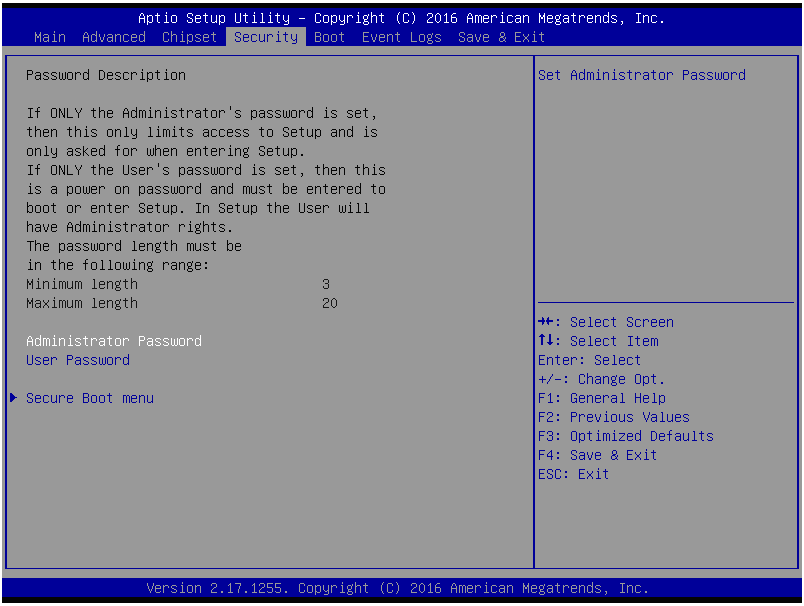
Control each of the USB ports disabling.

XHCI Idle L1

Enabled XHCI Idle L1. Disabled to workaround USB3 hot plug will fail after 1 hot plug removal.. Please put the system to G3 for the new settings to take effect.

8.5 Security Setup

Select the Security tab from the setup screen to enter the Security BIOS Setup screen. You can select any of Security BIOS Setup options by highlighting it using the < Arrow > keys. The Security BIOS Setup screen is shown below.



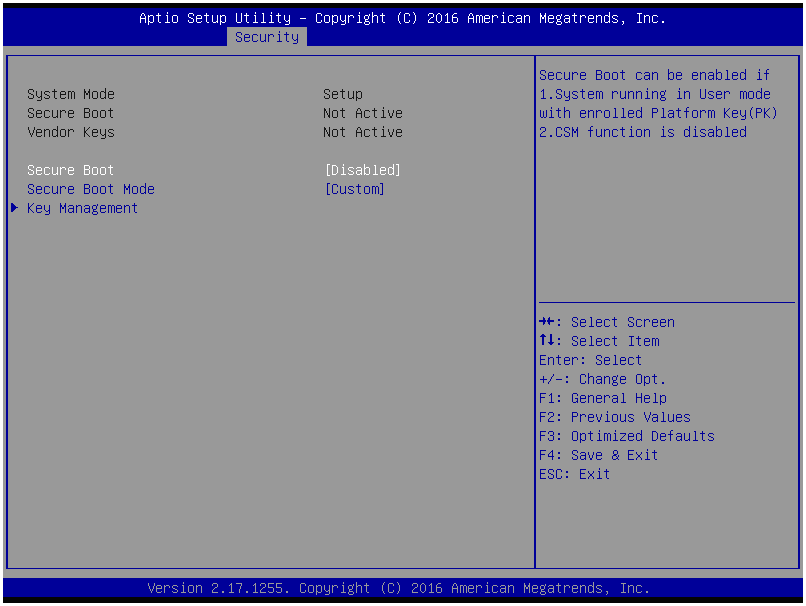
Administrator Password

Set Administrator Password.

User Password

Set User Password.

Secure Boot Menu



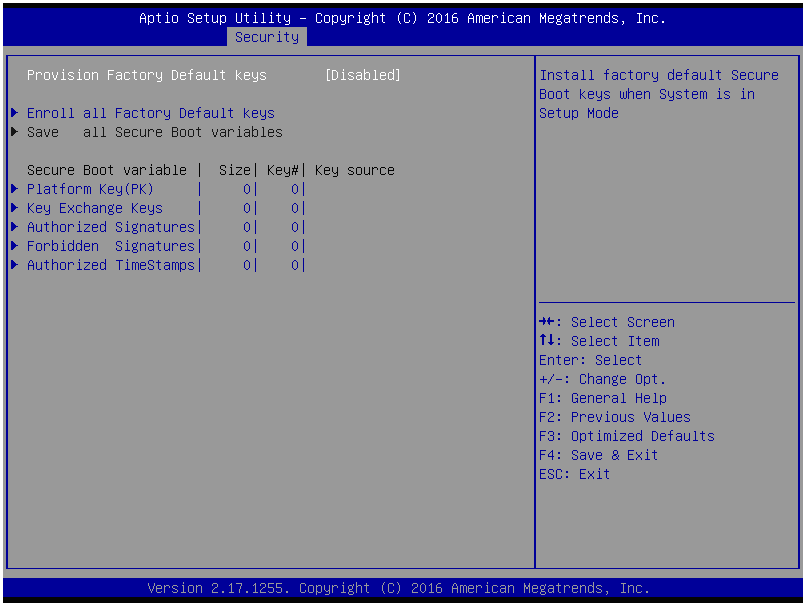
Secure Boot

Secure Boot can be enabled if 1.System running in User mode with enrolled Platform Key(PK) 2.CSM function is disabled.

Secure Boot Mode

Secure Boot mode selector. 'Custom' Mode enables users to change Image Execution policy and manage Secure Boot Keys.

Key Management



Provision Factory Default keys

Install factory default Secure Boot keys when System is in Setup Mode.

Enroll all Factory Default keys

Force System to User Mode - install all Factory Default keys (PK, KEK, db, dbt, dbx). Change takes effect after reboot.

Save all Secure boot variables

Save NVRAM content of all Secure Boot variables to the files (EFI_SIGNATURE_LIST data format) in root folder on a target file system device.

Platform Key (PK)

Enroll Factory Defaults or load the keys from a file with:

1. Public Key Certificate in: (a) EFI_SIGNATURE_LIST,
(b) EFI_CERT_X509 (DER encoded),
(c) EFI_CERT_RSA2048 (bin), (d) EFI_CERT_SHA256 (bin)

2. Authenticated UEFI Variable Key source: Default, Custom, Mixed(*) modified from Setup menu.

Key Exchange Keys

Enroll Factory Defaults or load the keys from a file with:

1. Public Key Certificate in: (a) EFI_SIGNATURE_LIST,
(b) EFI_CERT_X509 (DER encoded),
(c) EFI_CERT_RSA2048 (bin), (d) EFI_CERT_SHA256 (bin)

2. Authenticated UEFI Variable Key source: Default, Custom, Mixed(*) modified from Setup menu.

Authorized Signatures

Enroll Factory Defaults or load the keys from a file with:

1. Public Key Certificate in: (a) EFI_SIGNATURE_LIST,
(b),EFI_CERT_X509 (DER encoded),
(c) EFI_CERT_RSA2048 (bin), (d)EFI_CERT_SHA256 (bin)

2. Authenticated UEFI Variable Key source: Default, Custom, Mixed(*) modified from Setup menu.

Forbidden Signatures

Enroll Factory Defaults or load the keys from a file with:

1. Public Key Certificate in: (a) EFI_SIGNATURE_LIST,
(b) EFI_CERT_X509 (DER encoded),
(c) EFI_CERT_RSA2048 (bin), (d)EFI_CERT_SHA256 (bin)

2. Authenticated UEFI Variable Key source: Default, Custom, Mixed(*) modified from Setup menu.

Authorized Time Stamps

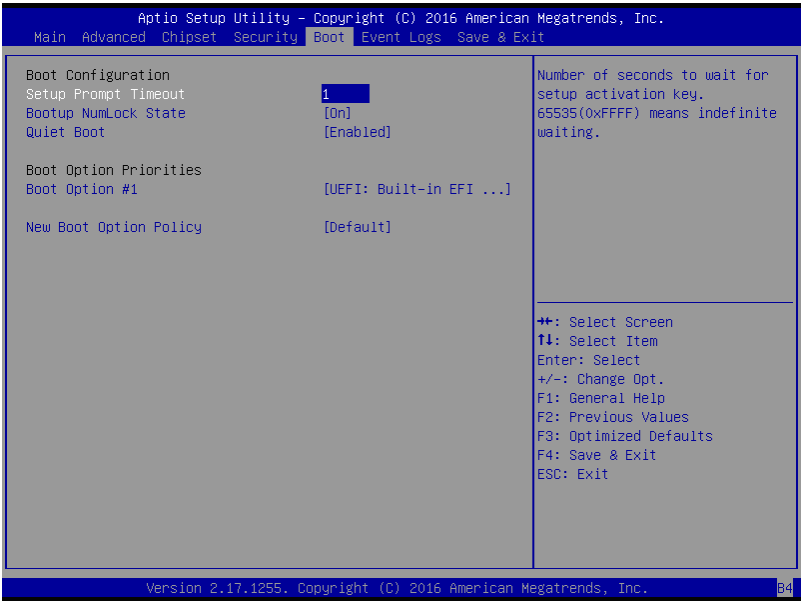
Enroll Factory Defaults or load the keys from a file with:

1. Public Key Certificate in: (a) EFI_SIGNATURE_LIST,
(b) EFI_CERT_X509 (DER encoded),
(c) EFI_CERT_RSA2048 (bin), (d)EFI_CERT_SHA256 (bin)

2. Authenticated UEFI Variable Key source: Default, Custom, Mixed(*) modified from Setup menu.

8.6 Boot Settings

Select the Boot tab from the setup screen to enter the Boot BIOS Setup screen. You can select any of the items in the left frame of the screen to go to the sub menu for that item. You can display a Boot BIOS Setup option by highlighting it using the < Arrow > keys. The Boot Settings screen is shown below:



Setup Prompt Timeout

Number of seconds to wait for setup activation key. 65535(0xFFFF) means indefinite waiting.

Bootup NumLock State

Select the keyboard NumLock state.

Quiet Boot

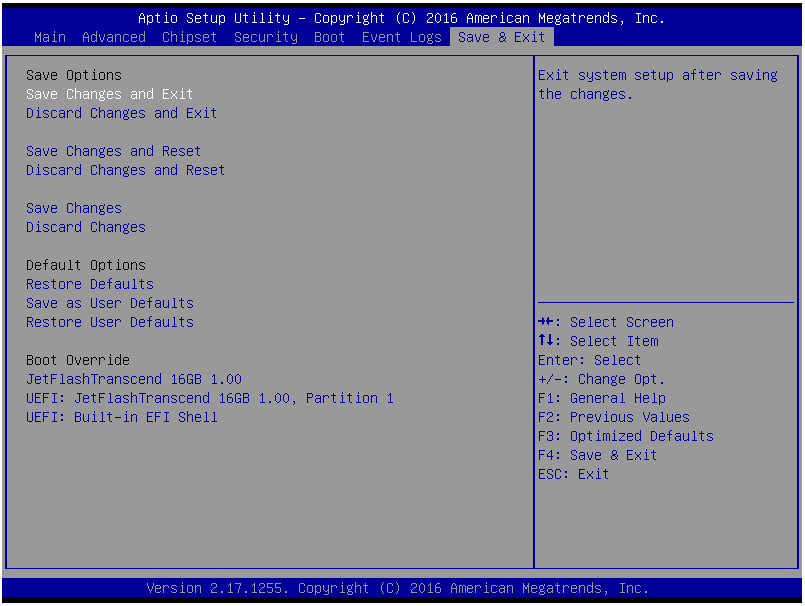
Enables or disables Quiet Boot option.

New Boot Option Policy

Controls the placement of newly detected UEFI boot options.

8.7 Save & Exit Menu

Select the Save & Exit tab from the setup screen to enter the Save & Exit BIOS Setup screen. You can display any Save & Exit BIOS Setup option by highlighting it using the < Arrow > keys. The Save & Exit BIOS Setup screen is shown below.



Save Changes and Exit

Exit the system after saving the changes.

Discard Changes and Exit

Exit system setup without saving any changes.

Save Changes and Reset

Reset the system after saving the changes.

Discard Changes and Reset

Reset system setup without saving any changes.

Save Changes

Save changes done so far to any of the setup options.

Discard Changes

Discard changes done so far to any of the setup options.

Restore Changes

Restore/Load Defaults values for all the setup options.

Save as User Defaults

Save the changes done so far as user defaults..

Restore User Defaults

Save changes done so far to any of the setup options.

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9 Checkpoints & Beep Codes

The eight User LEDs on the front panel display port 80h POST codes in hexadecimal during boot up. Users can use the POST codes to identify issues during the BIOS POST process (see See “User LEDs” on page 26.).

Below are the BIOS checkpoints and beep codes for the cPCI-6940. For assistance interpreting these codes, please login to **http://askanexpert.adlinktech.com**.

9.1 Checkpoint Ranges

Status Code Range	Description
0x01 – 0x0B	SEC execution
0x0C – 0x0F	SEC errors
0x10 – 0x2F	PEI execution up to and including memory detection
0x30 – 0x4F	PEI execution after memory detection
0x50 – 0x5F	PEI errors
0x60 – 0x8F	DXE execution up to BDS
0x90 – 0xCF	BDS execution
0xD0 – 0xDF	DXE errors
0xE0 – 0xE8	S3 Resume (PEI)
0xE9 – 0xEF	S3 Resume errors (PEI)
0xF0 – 0xF8	Recovery (PEI)
0xF9 – 0xFF	Recovery errors (PEI)

9.2 Standard Checkpoints

SEC Phase

Status Code	Description
0x00	Not used
Progress Codes	
0x01	Power on. Reset type detection (soft/hard).

Status Code	Description
0x02	AP initialization before microcode loading
0x03	North Bridge initialization before microcode loading
0x04	South Bridge initialization before microcode loading
0x05	OEM initialization before microcode loading
0x06	Microcode loading
0x07	AP initialization after microcode loading
0x08	North Bridge initialization after microcode loading
0x09	South Bridge initialization after microcode loading
0x0A	OEM initialization after microcode loading
0x0B	Cache initialization
SEC Error Codes	
0x0C – 0x0D	Reserved for future AMI SEC error codes
0x0E	Microcode not found
0x0F	Microcode not loaded

SEC Beep Codes

None

PEI Phase

Status Code	Description
Progress Codes	
0x10	PEI Core is started
0x11	Pre-memory CPU initialization is started
0x12	Pre-memory CPU initialization (CPU module specific)
0x13	Pre-memory CPU initialization (CPU module specific)
0x14	Pre-memory CPU initialization (CPU module specific)
0x15	Pre-memory North Bridge initialization is started

Status Code	Description
0x16	Pre-Memory North Bridge initialization (North Bridge module specific)
0x17	Pre-Memory North Bridge initialization (North Bridge module specific)
0x18	Pre-Memory North Bridge initialization (North Bridge module specific)
0x19	Pre-memory South Bridge initialization is started
0x1A	Pre-memory South Bridge initialization (South Bridge module specific)
0x1B	Pre-memory South Bridge initialization (South Bridge module specific)
0x1C	Pre-memory South Bridge initialization (South Bridge module specific)
0x1D – 0x2A	OEM pre-memory initialization codes
0x2B	Memory initialization. Serial Presence Detect (SPD) data reading
0x2C	Memory initialization. Memory presence detection
0x2D	Memory initialization. Programming memory timing information
0x2E	Memory initialization. Configuring memory
0x2F	Memory initialization (other).
0x30	Reserved for ASL (see ASL Status Codes section below)
0x31	Memory Installed
0x32	CPU post-memory initialization is started
0x33	CPU post-memory initialization. Cache initialization
0x34	CPU post-memory initialization. Application Processor(s) (AP) initialization
0x35	CPU post-memory initialization. Boot Strap Processor (BSP) selection
0x36	CPU post-memory initialization. System Management Mode (SMM) initialization
0x37	Post-Memory North Bridge initialization is started

Status Code	Description
0x38	Post-Memory North Bridge initialization (North Bridge module specific)
0x39	Post-Memory North Bridge initialization (North Bridge module specific)
0x3A	Post-Memory North Bridge initialization (North Bridge module specific)
0x3B	Post-Memory South Bridge initialization is started
0x3C	Post-Memory South Bridge initialization (South Bridge module specific)
0x3D	Post-Memory South Bridge initialization (South Bridge module specific)
0x3E	Post-Memory South Bridge initialization (South Bridge module specific)
0x3F-0x4E	OEM post memory initialization codes
0x4F	DXE IPL is started
PEI Error Codes	
0x50	Memory initialization error. Invalid memory type or incompatible memory speed
0x51	Memory initialization error. SPD reading has failed
0x52	Memory initialization error. Invalid memory size or memory modules do not match.
0x53	Memory initialization error. No usable memory detected
0x54	Unspecified memory initialization error.
0x55	Memory not installed
0x56	Invalid CPU type or Speed
0x57	CPU mismatch
0x58	CPU self test failed or possible CPU cache error
0x59	CPU micro-code is not found or micro-code update is failed
0x5A	Internal CPU error
0x5B	reset PPI is not available
0x5C-0x5F	Reserved for future AMI error codes

Status Code	Description
S3 Resume Progress Codes	
0xE0	S3 Resume is stared (S3 Resume PPI is called by the DXE IPL)
0xE1	S3 Boot Script execution
0xE2	Video repost
0xE3	OS S3 wake vector call
0xE4-0xE7	Reserved for future AMI progress codes
S3 Resume Error Codes	
0xE8	S3 Resume Failed
0xE9	S3 Resume PPI not Found
0xEA	S3 Resume Boot Script Error
0xEB	S3 OS Wake Error
0xEC-0xEF	Reserved for future AMI error codes
Recovery Progress Codes	
0xF0	Recovery condition triggered by firmware (Auto recovery)
0xF1	Recovery condition triggered by user (Forced recovery)
0xF2	Recovery process started
0xF3	Recovery firmware image is found
0xF4	Recovery firmware image is loaded
0xF5-0xF7	Reserved for future AMI progress codes
Recovery Error Codes	
0xF8	Recovery PPI is not available
0xF9	Recovery capsule is not found
0xFA	Invalid recovery capsule
0xFB – 0xFF	Reserved for future AMI error codes

PEI Beep Codes

# of Beeps	Description
1	Memory not Installed
1	Memory was installed twice (InstallPeiMemory routine in PEI Core called twice)
2	Recovery started
3	DXEIPL was not found
3	DXE Core Firmware Volume was not found
4	Recovery failed
4	S3 Resume failed
7	Reset PPI is not available

DXE Phase

Status Code	Description
0x60	DXE Core is started
0x61	NVRAM initialization
0x62	Installation of the South Bridge Runtime Services
0x63	CPU DXE initialization is started
0x64	CPU DXE initialization (CPU module specific)
0x65	CPU DXE initialization (CPU module specific)
0x66	CPU DXE initialization (CPU module specific)
0x67	CPU DXE initialization (CPU module specific)
0x68	PCI host bridge initialization
0x69	North Bridge DXE initialization is started
0x6A	North Bridge DXE SMM initialization is started
0x6B	North Bridge DXE initialization (North Bridge module specific)
0x6C	North Bridge DXE initialization (North Bridge module specific)
0x6D	North Bridge DXE initialization (North Bridge module specific)
0x6E	North Bridge DXE initialization (North Bridge module specific)

Status Code	Description
0x6F	North Bridge DXE initialization (North Bridge module specific)
0x70	South Bridge DXE initialization is started
0x71	South Bridge DXE SMM initialization is started
0x72	South Bridge devices initialization
0x73	South Bridge DXE Initialization (South Bridge module specific)
0x74	South Bridge DXE Initialization (South Bridge module specific)
0x75	South Bridge DXE Initialization (South Bridge module specific)
0x76	South Bridge DXE Initialization (South Bridge module specific)
0x77	South Bridge DXE Initialization (South Bridge module specific)
0x78	ACPI module initialization
0x79	CSM initialization
0x7A – 0x7F	Reserved for future AMI DXE codes
0x80 – 0x8F	OEM DXE initialization codes
0x90	Boot Device Selection (BDS) phase is started
0x91	Driver connecting is started
0x92	PCI Bus initialization is started
0x93	PCI Bus Hot Plug Controller Initialization
0x94	PCI Bus Enumeration
0x95	PCI Bus Request Resources
0x96	PCI Bus Assign Resources
0x97	Console Output devices connect
0x98	Console input devices connect
0x99	Super IO Initialization
0x9A	USB initialization is started
0x9B	USB Reset
0x9C	USB Detect
0x9D	USB Enable
0x9E – 0x9F	Reserved for future AMI codes

Status Code	Description
0xA0	IDE initialization is started
0xA1	IDE Reset
0xA2	IDE Detect
0xA3	IDE Enable
0xA4	SCSI initialization is started
0xA5	SCSI Reset
0xA6	SCSI Detect
0xA7	SCSI Enable
0xA8	Setup Verifying Password
0xA9	Start of Setup
0xAA	Reserved for ASL (see ASL Status Codes section below)
0xAB	Setup Input Wait
0xAC	Reserved for ASL (see ASL Status Codes section below)
0xAD	Ready To Boot event
0xAE	Legacy Boot event
0xAF	Exit Boot Services event
0xB0	Runtime Set Virtual Address MAP Begin
0xB1	Runtime Set Virtual Address MAP End
0xB2	Legacy Option ROM Initialization
0xB3	System Reset
0xB4	USB hot plug
0xB5	PCI bus hot plug
0xB6	Clean-up of NVRAM
0xB7	Configuration Reset (reset of NVRAM settings)
0xB8 – 0xBF	Reserved for future AMI codes
0xC0 – 0xCF	OEM BDS initialization codes
DXE Error Codes	
0xD0	CPU initialization error
0xD1	North Bridge initialization error
0xD2	South Bridge initialization error

Status Code	Description
0xD3	Some of the Architectural Protocols are not available
0xD4	PCI resource allocation error. Out of Resources
0xD5	No Space for Legacy Option ROM
0xD6	No Console Output Devices are found
0xD7	No Console Input Devices are found
0xD8	Invalid password
0xD9	Error loading Boot Option (LoadImage returned error)
0xDA	Boot Option is failed (StartImage returned error)
0xDB	Flash update is failed
0xDC	Reset protocol is not available

DXE Beep Codes

# of Beeps	Description
1	Invalid password
4	Some of the Architectural Protocols are not available
5	No Console Output Devices are found
5	No Console Input Devices are found
6	Flash update is failed
7	Reset protocol is not available
8	Platform PCI resource requirements cannot be met

ACPI/ASL Checkpoints

Status Code	Description
0x01	System is entering S1 sleep state
0x02	System is entering S2 sleep state
0x03	System is entering S3 sleep state
0x04	System is entering S4 sleep state
0x05	System is entering S5 sleep state
0x10	System is waking up from the S1 sleep state
0x20	System is waking up from the S2 sleep state
0x30	System is waking up from the S3 sleep state
0x40	System is waking up from the S4 sleep state
0xAC	System has transitioned into ACPI mode. Interrupt controller is in PIC mode.
0x72	System is entering S5 sleep statue.
0x84 (xhci mode enabled)	System has transitioned into ACPI mode. Interrupt controller is in PIC mode.
0x84 (xhci mode enabled)	System has transitioned into ACPI mode. Interrupt controller is in APIC mode.
0x83 (xhci mode disabled)	System has transitioned into ACPI mode. Interrupt controller is in PIC mode.
0x83 (xhci mode disabled)	System has transitioned into ACPI mode. Interrupt controller is in APIC mode.
0xAA	System has transitioned into ACPI mode. Interrupt controller is in APIC mode.

9.3 OEM-Reserved Checkpoint Ranges

Status Code	Description
0x05	OEM SEC initialization before microcode loading
0x0A	OEM SEC initialization after microcode loading
0x1D – 0x2A	OEM pre-memory initialization codes
0x3F – 0x4E	OEM PEI post memory initialization codes
0x80 – 0x8F	OEM DXE initialization codes
0xC0 – 0xCF	OEM BDS initialization codes

10 IPMI User Guide

10.1 Introduction

This chapter is written for those who already have a basic understanding of the newest implementation of the baseboard management controller (BMC) of the Intelligent Platform Management Interface (IPMI) specification rev. 2.0. It also describes the OEM extension IPMI command usages which are not listed in the IPMI specification.

10.2 Summary of Commands Supported by BMR-AVR-cPCI

The table below lists all the commands supported by the IPMC. The right most column indicates if a particular command is mandatory or optional for PICMG 3.0/2.9.

Command	IPMI Spec	NetFn	CMD	Description (Required by PICMG 3.0/2.9)
IPM Device "Global" Commands				
Get Device ID	20.1	App	01h	This command is used to retrieve the Intelligent Device's Hardware Revision, Firmware/Software Revision, and Sensor and Event Interface Command specification revision information.
Cold Reset	20.2	App	02h	This command directs the Responder to perform a 'Cold Reset' of itself. (Optional/Optional)
Warm Reset	20.3	App	03h	This command directs the Responder to perform a 'Warm Reset' of itself.
Get Self Test Results	20.4	App	04h	This command directs the device to return its Self Test results, if any. (Mandatory/Mandatory)

Command	IPMI Spec	NetFn	CMD	Description (Required by PICMG 3.0/2.9)
Get Device GUID	20.8	App	08h	This command returns a GUID (Globally Unique ID), also referred to as a UUID (Universally Unique IDentifier), for the management controller. (Optional/Optional)
Broadcast "Get Device ID"	20.9	App	01h	This is a broadcast version of the 'Get Device ID' command that is provided for the 'discovery' of Intelligent Devices on the IPMB. (Mandatory/Mandatory)
IPMI Messaging Support Commands				
Send Message	22.7	App	34h	The *Send Message* command is used for bridging IPMI messages between channels, and between the system management software (SMS) and a given channel. (Optional/Optional)
BMC Watchdog Timer				
Reset Watchdog Timer	27.5	App	22h	The *Reset Watchdog Timer* command is used for starting and restarting the Watchdog Timer from the initial countdown value that was specified in the *Set Watchdog Timer* command. (Mandatory/Optional)
Set Watchdog Timer	27.6	App	24h	The *Set Watchdog Timer* command is used for initializing and configuring the watchdog timer. The command is also used for stopping the timer. (Mandatory/Optional)
Get Watchdog Timer	27.7	App	25h	This command retrieves the current settings and present countdown of the watchdog timer. (Mandatory/Optional)
Event Commands				
Set Event Receiver	29.1	S/E	00h	This global command tells a controller where to send Event Messages. (Mandatory/Optional)

Command	IPMI Spec	NetFn	CMD	Description (Required by PICMG 3.0/2.9)
Get Event Receiver	29.2	S/E	01h	This global command is used to retrieve the present setting for the Event Receiver Slave Address and LUN. This command is only applicable to management controllers that act as IPMB Event Generators. (Mandatory/Optional)
Platform Event Message	29.3	S/E	02h	This command may be thought of as a request for the BMC to process the event data that the command contains. Typically, the data will be logged to the System Event Log (SEL). (Mandatory/Optional)
Sensor Device Commands				
Get Device SDR Info	35.2	S/E	20h	This command returns general information about the collection of sensors in a Dynamic Sensor Device. (Mandatory/Optional)
Get Device SDR	35.3	S/E	21h	The 'Get Device SDR' command allows SDR information for sensors for a Sensor Device (typically implemented in a satellite management controller) to be returned. (Mandatory/Optional)
Reserve Device SDR Repository	35.4	S/E	22h	This command is used to obtain a *Reservation ID*. (Mandatory/Optional)
Set Sensor Hysteresis	35.6	S/E	24h	This command provides a mechanism for setting the hysteresis values associated with the thresholds of a sensor that has threshold based event generation. (Optional/Optional)
Get Sensor Hysteresis	35.7	S/E	25h	This command retrieves the present hysteresis values for the specified sensor. (Optional/Optional)
Set Sensor Threshold	35.8	S/E	26h	This command is used to set the specified threshold for the given sensor. (Optional/Optional)
Get Sensor Threshold	35.9	S/E	27h	This command retrieves the threshold for the given sensor. (Optional/Optional)

Command	IPMI Spec	NetFn	CMD	Description (Required by PICMG 3.0/2.9)
Set Sensor Event Enable	35.10	S/E	28h	This command provides the ability to disable or enable Event Message Generation for individual sensor events. The command is also used to enable or disable sensors in their entirety using the *disable scanning* bit. (Optional/Optional)
Get Sensor Event Enable	35.11	S/E	29h	This command returns the enabled/ disabled state for Event Message Generation from the selected sensor. The command also returns the enabled/ disabled state for scanning on the sensor. (Optional/Optional)
Get Sensor Event Status	35.13	S/E	2Bh	The Get Sensor Event Status command is provided to support systems where sensor polling is used in addition to, or instead of, Event Messages for event detection. (Optional/Optional)
Get Sensor Reading	35.14	S/E	2Dh	This command returns the present reading for sensor. The sensor device may return a stored version of a periodically updated reading, or the sensor device may scan to obtain the reading after receiving the request. (Mandatory/Optional)
Get Sensor Type	35.16	S/E	2Fh	This command is used to assign the Sensor Type and Event/Reading Type to a specified sensor. (Optional/Optional)
FRU Device Commands				
Get FRU Inventory Area Info	34.1	Storage	10h	Returns overall the size of the FRU Inventory Area in this device, in bytes. (Mandatory/Optional)
Read FRU Data	34.2	Storage	11h	The command returns the specified data from the FRU Inventory Info area. (Mandatory/Optional)
Write FRU Data	34.3	Storage	12h	The command writes the specified byte or word to the FRU Inventory Info area. (Mandatory/Optional)

10.3 CompactPCI Address Map

Since more than one system may be installed in a single chassis, we allocate each IPMB address based on GA input as peripheral cards. The CompactPCI Peripheral Address Mapping Table is given below.

CompactPCI Peripheral Address Mapping			
Geo. Addr.	**IPMB Addr.**	**Geo. Addr.**	**IPMB Addr.**
0	**Disabled**	16	D0h
1	B0h	17	D2h
2	B2h	18	D4h
3	B4h	19	D6h
4	B6h	20	D8h
5	B8h	21	DAh
6	Bah	22	DCh
7	BCh	23	DEh
8	BEh	24	E0h
9	Coh	25	E2h
10	C4h	26	E4h
11	C6h	27	E6h
12	C8h	28	E8h
13	CAh	29	EAh
14	CCh	30	ECh
15	CEh	**31**	**Disabled**

10.4 Communications with IPMC

Operating systems need to use a serial port to communicate with the IPMC. The resource setting of the serial port must be IO: 0x3F8 and IRQ: 4. The communication setting of the serial port must be BaudRate: 9600, DataBit: 8, ParityCheck: None, StopBit: 1, and FlowControl: None.

10.5 IPMI Sensors List

Sensor Number	Sensor name	Normal Reading	Sensor Reading Value of IPMI Get Sensor Reading Command
01h	BMC Watchdog		Timeout action: 000b = no action 001b = Hard Reset 000b = Power Down 011b = Power Cycle 100b - 111b = reserved
02h	+1.0V	1.0 V	Raw data of 1.0V sensor
03h	+1.05V PCH	1.05 V	Raw data of 1.05V sensor
04h	+1.35V	1.35 V	Raw data of 1.35V sensor
05h	+0.675V	0.675 V	Raw data of 0.675V sensor
06h	+1.5V	1.5 V	Raw data of 1.5V sensor
07h	+1.8V BG	1.8 V	Raw data of 1.8V sensor
08h	+12V STB	12 V	Raw data of 12V sensor
09h	VCORE	1.6 V -1.8 V	Raw data of 1.6V – 1.8V sensor
0Ah	+1.8 SA	1.8 V	Raw data of 1.8V sensor
0Bh	+3.3V	3.3 V	Raw data of 3.3V sensor
0Ch	+5.0V L	5.0 V	Raw data of 5.0V sensor
0Dh	+3.3V STB	3.3 V	Raw data of 3.3V sensor
0Eh	+3.3V_W	11 W	Raw data of 11W sensor
0Fh	+5V_W	23 W	Raw data of 23W sensor
10h	CPU Temp	40ºC	Raw data of CPU Temp sensor
11h	SYSTEM Temp	25ºC	Raw data of SYSTEM Temp sensor

10.6 Relevant Documents

Document Title	Revision	Source
Intelligent Platform Management Interface Specification v2.0	Document Revision 1.0 February 12, 2004	Intel Corp. http://www.intel.com/design/servers/ipmi/spec.htm
PICMG 2.9 D1.0 CompactPCI System Management Specification	January 21, 2000	
Intelligent Platform Management Bus Communications Protocol Specification v0.9	Document Revision 0.15 June 24, 1997	Intel Corp. http://www.intel.com/design/servers/ipmi/license_ipmi.htm

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Important Safety Instructions

For user safety, please read and follow all **instructions**, **WARNINGS**, **CAUTIONS,** and **NOTES** marked in this manual and on the associated equipment before handling/operating the equipment.

- Read these safety instructions carefully.
- Keep this user's manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- When installing/mounting or uninstalling/removing equipment:
  - Turn off power and unplug any power cords/cables.
- To avoid electrical shock and/or damage to equipment:
  - Keep equipment away from water or liquid sources;
  - Keep equipment away from high heat or high humidity;
  - Keep equipment properly ventilated (do not block or cover ventilation openings);
  - Make sure to use recommended voltage and power source settings;
  - Always install and operate equipment near an easily accessible electrical socket-outlet;
  - Secure the power cord (do not place any object on/over the power cord);
  - Only install/attach and operate equipment on stable surfaces and/or recommended mountings; and,
  - If the equipment will not be used for long periods of time, turn off and unplug the equipment from its power source.

- Never attempt to fix the equipment. Equipment should only be serviced by qualified personnel.

A Lithium-type battery may be provided for uninterrupted, backup or emergency power.

Risk of explosion if battery is replaced with one of an incorrect type. Dispose of used batteries appropriately.

- Equipment must be serviced by authorized technicians when:
  - The power cord or plug is damaged;
  - Liquid has penetrated the equipment;
  - It has been exposed to high humidity/moisture;
  - It is not functioning or does not function according to the user's manual;
  - It has been dropped and/or damaged; and/or,
  - It has an obvious sign of breakage.

Getting Service

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