

# PCIe/PXIe-9852

## 2-CH 14-Bit 200 MS/s High-Speed PCI Express/PXI Express Digitizers



### Introduction

The ADLINK PCIe/PXIe-9852 is a 2-CH 14-bit 200 MS/s digitizer for high frequency and wide dynamic range signals with an input frequency up to 90 MHz. The 90 MHz bandwidth analog input with 50 $\Omega$  impedance is designed to receive  $\pm 0.2$  V,  $\pm 2$  V, or  $\pm 10$  V high speed signals. With a PCI Express bus interface and ample onboard acquisition memory up to 1 GB, the PCIe/PXIe-9852 easily manages simultaneous 2-CH data streaming. With high speed and high linearity 14-bit A/D converters and high stable onboard reference, the PCIe/PXIe-9852 provides both high accuracy and high dynamic performance, making it ideal for applications requiring high-speed data acquisition, such as optical fiber and LIDAR testing, and video signal analysis.

### Highlights

#### Data Streaming Up to 800MB/s

Based on PCI Express Gen2 technology, the PCIe/PXIe-9852 can stream data on both channels at its maximum data rate (200 MS/s), and continuously stream data to the host PC at rates up to 800 MB/s. An 8 x 500 GB driver RAID system (4TB) extends capture sessions to more than one hour.

#### Onboard Signal Averaging Technology

Every PCIe/PXIe-9852 provides onboard Signal Averaging, allowing detection of small repetitive signals in noisy environments with no CPU loading, suitable for applications requiring extraction of small signals from background noise such as optical fiber testing.

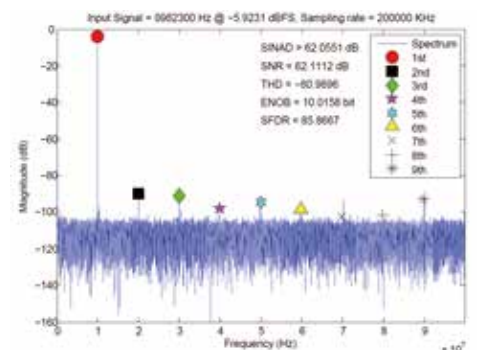
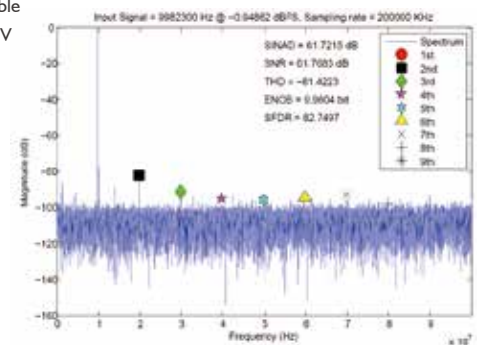
### Features

- PCI Express specification Rev. 2.0 compliant (PCIe-9852)
- PXI Express specification Rev. 1.0 compliant (PXIe-9852)
- Up to 200 MS/s sampling rate
- 2 simultaneous analog inputs
- High resolution 14-bit ADC
- Up to 90 MHz bandwidth for analog input
- 1 GB onboard storage memory
- Programmable input voltage range of  $\pm 0.2$  V,  $\pm 2$  V, or  $\pm 10$  V
- Scatter-gather DMA data transfer for high speed data streaming
- One external digital trigger input and one external trigger output
- One external clock input
- Full auto-calibration
- Supports signal averaging
- Supported Operating System
  - Windows 7/8 x64/x86, Linux
- Driver and SDK
  - LabVIEW, MATLAB, C/C++, Visual Basic, Visual Studio.NET

### Specifications

#### Analog Input

- Number of Channels: 2 single-ended
- Input Coupling: AC or DC, software selectable
- AC coupling cutoff frequency: 11 Hz
- -3 dB Bandwidth: 90MHz
- Input Impedance: 50 $\Omega$  or 1M $\Omega$ , software selectable
- Input Signal Range: Range:  $\pm 0.2$  V,  $\pm 2$  V, or  $\pm 10$  V
- Overvoltage Protection:
  - with 50 $\Omega$  :  $\pm 10$ V sine wave, 7Vrms
  - with 1M $\Omega$  :  $\pm 10$ V
- ADC Resolution: 14 bits, 1 in 16384
- Gain Error:  $\pm 0.65\%$  of input
- Offset error:  $\pm 1$  mV
- Crosstalk: < -80 dB
- Spectral Characteristics
  - Input Range:  $\pm 0.2$  V
  - Sampling Rate: 200 MS/s
  - SINAD: 61.72 dBc
  - SNR: 61.77 dBc
  - THD: -81.42 dBc
  - ENOB: 9.96 bit
  - SFDR: 82.75 dBc
- Spectral Characteristics
  - Input Range:  $\pm 2$  V
  - Sampling Rate: 200 MS/s
  - SINAD: 62.06 dBc
  - SNR: 62.11 dBc
  - THD: -80.97 dBc
  - ENOB: 10.02 bit
  - SFDR: 85.87 dBc



### Trigger

- Trigger Source
  - Software
  - External digital
  - Analog inputs
  - SSI (PCIe-9852)
  - PXI\_STAR (PXIe-9852)
  - PXI\_trigger bus [0..7] (PXIe-9852)
  - PXIe\_DSTARB (PXIe-9852)
- Trigger Modes
  - Post-trigger
  - Pre-trigger
  - Middle trigger
  - Delay trigger
- External Digital Trigger Input
  - Source: Front panel SMA connector
  - Compatibility: 3.3V TTL, 5V tolerance
  - Input high threshold: 2.0 V
  - Input low threshold: 0.8V
  - Maximum input overload: -0.5V ~ +5.5V
  - Trigger polarity: Rising or falling edge, software programmable
  - Pulse width: 20 ns minimum
- External Digital Trigger Output
  - Compatibility: 5V TTL
  - Output high threshold: 2.4V
  - Output low threshold: 0.2V
  - Trigger polarity: Positive or negative
  - Pulse width: 50 ns, 100 ns, 150 ns, 200 ns, 1  $\mu$ s, 2  $\mu$ s, 7.5  $\mu$ s, and 10  $\mu$ s
  - Driving capacity: Capable of driving 50 $\Omega$  load

### Timebase

- Timebase options
  - Internal: onboard synthesizer
  - External: CLK IN (front panel)
- Sampling clock frequency
  - Internal: 200M Hz
  - External: 40M Hz ~ 200M Hz (CLK IN)
  - Timebase accuracy:  $< \pm 25$  ppm
- External reference clock source: Front panel, SSI (PCIe-9852), PXI\_CLK10 or PXIe\_CLK100 (PXIe-9852)
- External reference clock: 10M Hz or 100M Hz
- External reference clock input range: 500mVpp ~ 5Vpp (AC/DC compliant)
- External sampling clock input range: 1Vpp ~ 5Vpp (AC/DC compliant)

### Data Storage and Transfer

- 1 GB onboard memory, shared among the two analog inputs
- Scatter-Gather DMA data transfer

### Onboard Reference

- +5V and +2.5V onboard reference voltage
- $< 3.0$  ppm/ $^{\circ}$ C reference temperature drift
- 15 minutes recommended warmup

## Ordering Information

■ **PCIe-9852**  
2-CH 14-Bit 200 MS/s High-Speed PCI Express Digitizer

■ **PXIe-9852**  
2-CH 14-Bit 200 MS/s High-Speed PXI Express Digitizer

### General Specifications

- I/O Connector
  - SMA x 2 for analog inputs
  - SMA x 1 for external trigger input
  - SMA x 1 for external trigger output
  - SMA x 1 for external clock input
- Dimensions (not including connectors):
  - PCIe-9852 : 167.64 (W) x 106.68 (H) mm (6.53" x 4.16")
  - PXIe-9852 : 160 (W) x 100 (H) mm (6.24" x 3.9")
- Bus Interface: PCI Express Gen 2 x4
- Ambient Temperature (Operating):
  - PCIe-9852 : 0 $^{\circ}$ C to 50 $^{\circ}$ C (32 $^{\circ}$ F to 122 $^{\circ}$ F)
  - PXIe-9852 : 0 $^{\circ}$ C to 55 $^{\circ}$ C (32 $^{\circ}$ F to 131 $^{\circ}$ F)
- Ambient Temperature (Storage): -20 $^{\circ}$ C to 80 $^{\circ}$ C (-4 $^{\circ}$ F to 176 $^{\circ}$ F)
- Relative Humidity: 10% to 90%, non-condensing
- Power consumption:

Power Rail	Standby current (mA)	Full load (mA)
+3.3 V	102	102.2
+12 V	20	20
+5 V	1920	2010

### Certifications

- EMC/EMI: CE, FCC Class A

### IO connector definition

CLK IN  
TRG IN  
TRG OUT  
CH0  
CH1



### SSI Bus Cables (for multiple card synchronization)

#### ■ ACL-eSSI-2/3/4

SSI bus cable for two, three, and four devices

