

iSPAN™ 6535 T1/E1/J1 Communications Controller

The Industry's Most Advanced CompactPCI
Controller for Telecommunications

FEATURES

Motorola's MPC8260 (PowerQUICC II™) on-board processor, featuring:

- 200 MHz RISC CPU, 280 MIPS
- 64-bit, 66 MHz local data bus
- Up to 700 Mbps CPM protocol engine

64-bit, 33 MHz (upgradeable to 66 MHz) PCI bridge, supporting multiple transfer modes

64 MB SDRAM for high-performance, high-capacity local segmentation and reassembly

4 MB of downloadable Flash EPROM

8 MB of CPM connection memory

Both front and rear access (via passive Rear Transition Module) options available

Eight ports software selectable as T1/E1/J1 interfaces

One Fast Ethernet interface and mini-DIN TTY port (front panel)

Integrated CSU on T1 lines with support for Facility Data Link

Full hot swap capability

H.110 bus, 512 time slot local-to-H.110 bus, 1024 local-to-local time slots

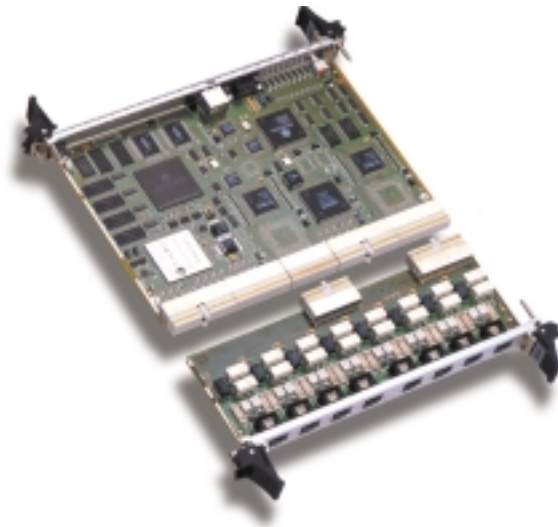
Support for ATM AAL0, AAL2 and AAL5 Adaptation Layers

Multiprotocol support for SS7, ATM, Frame Relay, X.25, ISDN HDLC and PPP

Optional Inverse Multiplexing for ATM (IMA)

On-board support for multiple types of voice and data traffic:

- Frame Relay and voice traffic over TDM
- Frame Relay conversion to IP over Ethernet
- Packetized voice
- SS7, ISDN, MTP1 and MTP2



Wireless Base Station BSCs/RNCs and BTSs/Node Bs
Internet Access Servers • Softswitches • Internet Gateway Devices
L2, L3 Switches • Internet IP Routers • AIN SCPs and IPs
Wireless Gateways • PSDNs • HLRs/VLRs • AAA Servers

The Internet and corporate global network infrastructures have changed the way that companies do business. The new world packet technologies, IP and ATM, have drastically increased the speed of connectivity and flexibility of services at greatly reduced costs and enabled a new generation of applications. In response, service providers are turning to equipment suppliers who provide cost-effective solutions that offer more functionality and faster time-to-market. Interphase designed the *iSPAN* 6535 to drive its customers to market faster with carrier-class hardware and software designed for the most demanding environments.

The Interphase *iSPAN* 6535 T1/E1/J1 Communications Controller sets the standard for high-performance and reliability as the industry's most advanced CompactPCI T1/E1/J1 communications controller for telecommunication applications. The 6535 outshines its competition with the industry's best performance, a comprehensive array of protocol and operating system support, and robust development tools to simplify the integration process. Featuring a powerful MPC8260 RISC on-board processor and support for multiple types of voice and data traffic, the 6535 allows for seamless migration to next generation infrastructures while preserving investments in legacy technologies.

Powerful Features for Next-Generation Telecommunications

6535 Architecture

The iSPAN 6535 CompactPCI T1/E1/J1 Communications Controller is the flagship product in the Interphase line of MPC8260-based communications controllers for carrier-class telecommunication environments. The software selectable interfaces for 8 T1/E1/J1 ports enable maximum flexibility to support multiple national variants with just one board.

The T1/E1/J1 framers feed DS0 traffic to an on-board H.110 TDM switch module, which then feeds multiple DS0s to the 8260 for internal processing or to the H.110 TDM bus for I/O to/from other slots. The T1/E1/J1 framers can also simultaneously feed any number of DS0s to the Inverse Multiplexer over ATM (IMA) chip on the 6535, which then aggregates the DS0s in full or fractional T1 streams into a single ATM pipe to be processed by the 8260's CPM.

With this powerful functionality, the 8260 Communications Processor Module (CPM) can simultaneously support multiple protocols including ATM, SS7, Frame Relay and others via the internal timeslot assigner and the internal UTOPIA bus interface. The 8260 CPM has access to its own 32-bit local bus, where the 32K entry look-up Content Addressable Memory (CAM) and 8 MB SDRAM are available for unimpeded read/write access to connection and routing tables.

The 8260 features a 64-bit, 66 MHz local data bus connecting up to 128 MB of SDRAM, up to 4 MB of boot code FLASH EPROM, and a 64-bit wide PowerSPAN® PCI bridge. The PowerSPAN bridge operates at 33 MHz (upgradeable to 66 MHz) on the backplane, supporting several DMA transfer modes for enhanced interprocess communications.

The 6535 is also equipped with a Fast Ethernet port on the faceplate. The 10/100 Base-T port supports full duplex 100 Mbps traffic, and therefore may be used for a variety of bridging/routing purposes, protocol interworking purposes, or simply to download/communicate with the 8260 CPU. A mini-DIN TTY port is also provided on the front panel.

Processor/Memory

- PowerQUICC II (MPC8260) 64-bit RISC processor allows full support of various communications protocols, reducing host CPU processing
 - Dual bus architecture: 64-bit 60x bus and 32-bit local CPM bus
 - 200 MHz core, 133 MHz CPM, 280 MIPS CPU
 - 64 MB or 32 MB 64-bit SDRAM memory
 - 4 MB downloadable 8-bit Flash EEPROM
 - 8 MB 32-bit Connection Memory



Line Interfaces

- Either four or eight individually software selectable front or rear access T1/E1/J1 interfaces (rear access via passive universal Rear Transition module)
- No component changes between T1, E1 or J1 terminations
- Each RJ-48C line is software configurable in Line Termination or Network Termination mode
- Integrated Channel Service Unit (CSU) in T1 mode
- Rear Transition Module includes line protections to comply with ETS300 046-3, UL1459, FCC68, and Bellcore TR-NWT-001089
- QuadFALC™ framer supports long haul or short haul interface, AMI, HDB3, or B8ZS line coding and various Super-Frame Formats
- One Fast Ethernet interface on the front panel for remote boot or LAN capability with 10/100 Base-T transceiver
- One mini-DIN TTY console port on front panel

CompactPCI Interfaces

The board is connected to the host through a CompactPCI compliant bus. This connection is done through CompactPCI connectors J1, J2, J4, and J5.

- Connector J1 is used for 32-bit PCI signals
- Connector J2 is used for 64-bit PCI signals
- Connector J4 is used for computer telephony bus compliant with the H.110 specification
- Connectors J3 and J5 are used for access to the Rear Transmission Module
- Hot Swappable

Telecom Clock Management

- The line interface can be configured in LT (clock slave) or NT (clock master) mode.
- Three line synchronization sources:
 - Free running internal clock
 - Recovered clock (loopback timing)
 - Network reference (via H.110 on J4)
- Recovered clock available on H.110 bus (J4)

On-Board H.110 Bus

The H.110 TDM bus on the 6535 controller allows multiple I/Os to share resources across multiple system slots:

- Enables services to expand to multiple slots within same chassis
- Up to 512 H.110-to-local timeslot switch capability
- Up to 1024 local-to-local timeslot switch capability

Inverse Multiplexing for ATM (IMA)

- Supports up to 8 T1, E1, or J1 lines into a single ATM pipe
- Allows a mix of IMA and non-multiplexed DS0 channels to co-exist on the same facilities (ex. IMA or fractional T1/E1/J1)
- Up to 4 IMA groups

Reduce Time-to-Market with Robust Software Development Tools

Interphase offers a robust suite of software development tools to help shorten the learning curve and design cycle for integration projects based on the 6535 communications controller. Because integrators and equipment providers have diverse development environments, Interphase provides three types of development tools, each tailored to the needs of different integration types. The Board Development Kit (BDK) facilitates development of device drivers, embedded protocol firmware and applications for the 6535 hardware module. The Board Support Package (BSP) allows software developers to write software applications that run on a specific operating system embedded on the MPC8260 CPU. The *iWARE*™ Software Development Suite offers developers a set of Interphase-developed firmware protocol stacks, accessible via APIs provided by Interphase.

Board Development Kit

The 6535 BDK is specific to the 6535 hardware, but it is not tied to a particular operating system environment.

The kit contains the following main components:

- **Setup Utility:** Allows the user to modify the content of the various programmable elements of the board, especially the Flash EEPROM memory.
- **Interactive Built-In Test Utility:** Allows management of the card such as, reset/run action, memory and register dump, memory and DMA tests, line parameter manipulation, and more.
- **Board Installation and Maintenance Manual:** Provides procedures for installing and maintaining the module.
- **Hardware Reference Manual:** Provides information for developing embedded software and/or host drivers for the module.
- **Built-in Self Test and Monitor Manual:** Provides high-level information for using the Boot Firmware.

Board Support Package

The 6535 Board Support Package consists of documentation compiled as a Board Support Guide for VxWorks. This document provides valuable information on how to configure and install VxWorks on the 6535. Once the BSP is installed, the 6535 can be connected to an Ethernet network and development can be done directly from the particular RTOS development environment, such as Tornado. The 6535 Board Support Package (BSP) also includes the files required to make an RTOS run embedded on the 6535 CPU.

The package provides source files for:

- TTY driver
- Ethernet driver (broadcast and multicast support)
- Interrupt controller
- Timestamp driver
- Auxiliary timer support
- Flash Memory Management
- True Flash File system (TFFS) support
- MMU support

iWARE Software Development Suite

The *iWARE* 6535 Software Development Suite reduces software development time and facilitates faster time to market by supplying embedded protocol support for ATM and SS7, base drivers for a selected operating system, configuration and diagnostic utilities, and sample programs.

The 6535 is initially offered with an *iWARE* 6535 Software Development Suite for Solaris 2.6, 2.7 and 2.8. The *iWARE* 6535 Software Development Suites enable easy integration and tools and diagnostics to enable faster time to market. The *iWARE* 6535 Software Development Suites also provide Interphase's own ATM and SS7 protocol support for SS7 MTP2, AAL0, AAL2, and AAL5, with ATM Quality of Service classes of service for Constant Bit Rate (CBR), Unspecified Bit Rate (UBR), and Variable Bit Rate (VBR).

The *iWARE* 6535 Software Development Suite supplied with the 6535 module consists of software programs and utilities running on the host CPU, and embedded software ("firmware") which runs on the on-board 8260 networking processor.

Software elements are separated into four modules:

- The base drivers for each supported Operating System (executed by the host processor)
- The configuration and diagnostic utilities
- Sample programs
- The embedded firmware executed by the 8260 on the 6535 board

These modules interact with each other through well-defined and documented interfaces. A common WAN API is defined at the interface between the embedded firmware and the various drivers.

A complete documentation set is also provided describing Interphase's *iWARE* WAN API (Wide Area Network Application Programmer's Interface), the Base Driver's API, sample programs, and tool guides.

iSPAN 6535 CompactPCI T1/E1/J1 Communications Controller

Industry Standards Compliance

PCI-SIG Peripheral Component Interconnect (PCI) Local Bus Specification, Rev 2.2
CompactPCI 2.1
CompactPCI PICMG 2.0 R3.0

Physical Layer 1 and Protocol Standards Compliance

ANSI T.403: Network and Customer Installations Interface - DS1 Electrical Interface
ANSI T.107: Digital Hierarchy Format Specification
AT&T TR 62411: Accunet T1.5 - Service description and Interface

Interface Specifications

Telcordia SR-4994 Layer 1, National ISDN Primary Rate
ITU-T G.703 General Aspects of Digital Transmission Systems
ITU-T G.704 General Aspects of Digital Transmission Systems
ANSI T1.403-1995
ANSI T1.107-1995
EIA 232-D Interface Between Data Terminal Equipment and Data Circuit-Terminating Equipment Employing Serial Binary Data Interchange
Bellcore TR-NWT-001089
IEEE 802.3: Fast Ethernet
Japanese references: ITU-JT G.703, ITU-JT G.704, ITU-JT G.706

Agency Certifications

Safety + EMC

- UL 1950
- UL 1459
- CSA/CAN C22.2 No. 950-95
- EN 60950
- IEC 60950 2nd Edition, 1991+Amd.1, 1992 + Amd.2, 1993 + Amd.3, 1995 + Amd.4, 1996
- ETS-300 046 Integrated Services Digital Network (ISDN); Primary rate access

Markings

- CE Mark

Interface

- FCC Part 68
- CS-03, Issue 8, Part II (Canada)

Emissions/Immunities

- FCC, Part 15, Class A
- ICES-003, Class A (Canada EMC)
- EN 55022; CISPR 22, Class A (Europe EMC)
- EN 55024; CISPR 24 (Europe Immunity)
- VCCI, Class A

SPECIFICATIONS

Architecture

Bus Type CompactPCI, H.110
Bus Access 32-bit, 33 MHz, can be configured
..... for 64-bit 66MHz
Processor 200MHz Motorola MPC8260
Memory 32/64MB SDRAM

Mechanical

Form Factor 6U CompactPCI
Length 266.7 mm
Width 215.9 mm
RTM Length 266.7 mm
RTM Width 134.5 mm

Operating Environment

Temperature 0 to 55° C
Relative Humidity 5% to 95% non-condensing
Altitude 0 to 15,000 ft
Power Consumption 5V: 1.7A, 3.3V: 2.0A

Software Support

iWARE Software Development Suite for Solaris
VxWorks Board Support Package (BSP)
Board Development Kit (BDK)

CONFIGURATION OPTIONS

The iSPAN 6535 CompactPCI T1/E1/J1 Communications Controller is available in the configurations listed below. Rear-access configurations include the Rear Transition Module.

6535-003: 8 T1/E1/J1 ports, 64 MB SDRAM, Rear Access

6535-004: 8 T1/E1/J1 ports with ATM/IMA, 64 MB SDRAM, Rear Access

6535-005: 8 T1/E1/J1 ports, 64 MB SDRAM, Front Access

6535-006: 8 T1/E1/J1 ports with ATM/IMA, 64 MB SDRAM, Front Access

6535-011: 8 T1/E1/J1 ports, 64 MB SDRAM, Rear Access, with keyed connectors on RTM

6535-012: 8 T1/E1/J1 ports with ATM/IMA, 64 MB SDRAM, Rear Access, with keyed connectors on RTM

6535-901: Board Support Package for VxWorks, unlimited use

6535-902: iWARE Software Development Suite for Solaris, one license/board

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